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THE MAGAZINE FOR QUALITY IN ELECTRONICS

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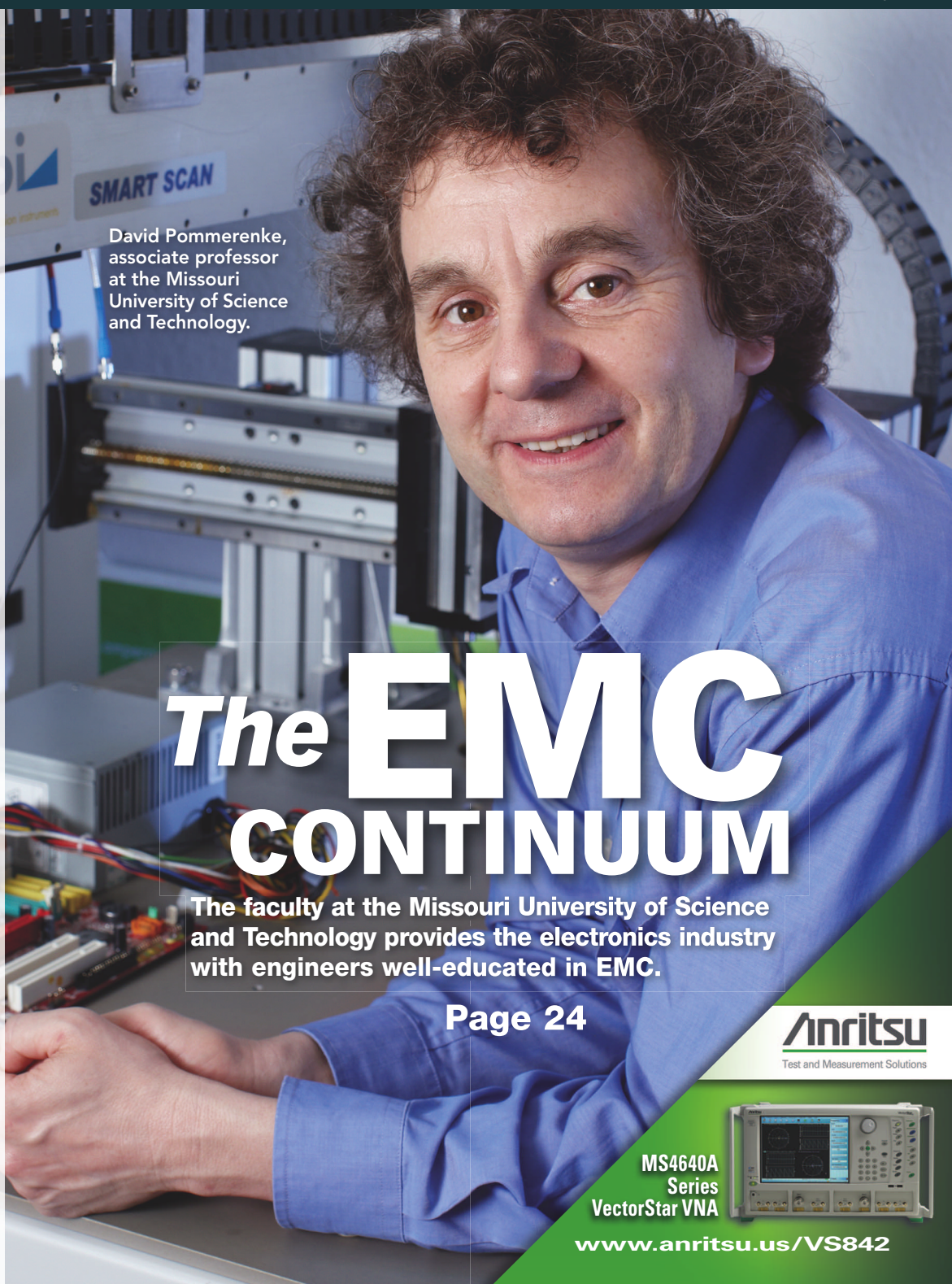

David Pommerenke, associate professor at the Missouri University of Science and Technology.

The EMC CONTINUUM

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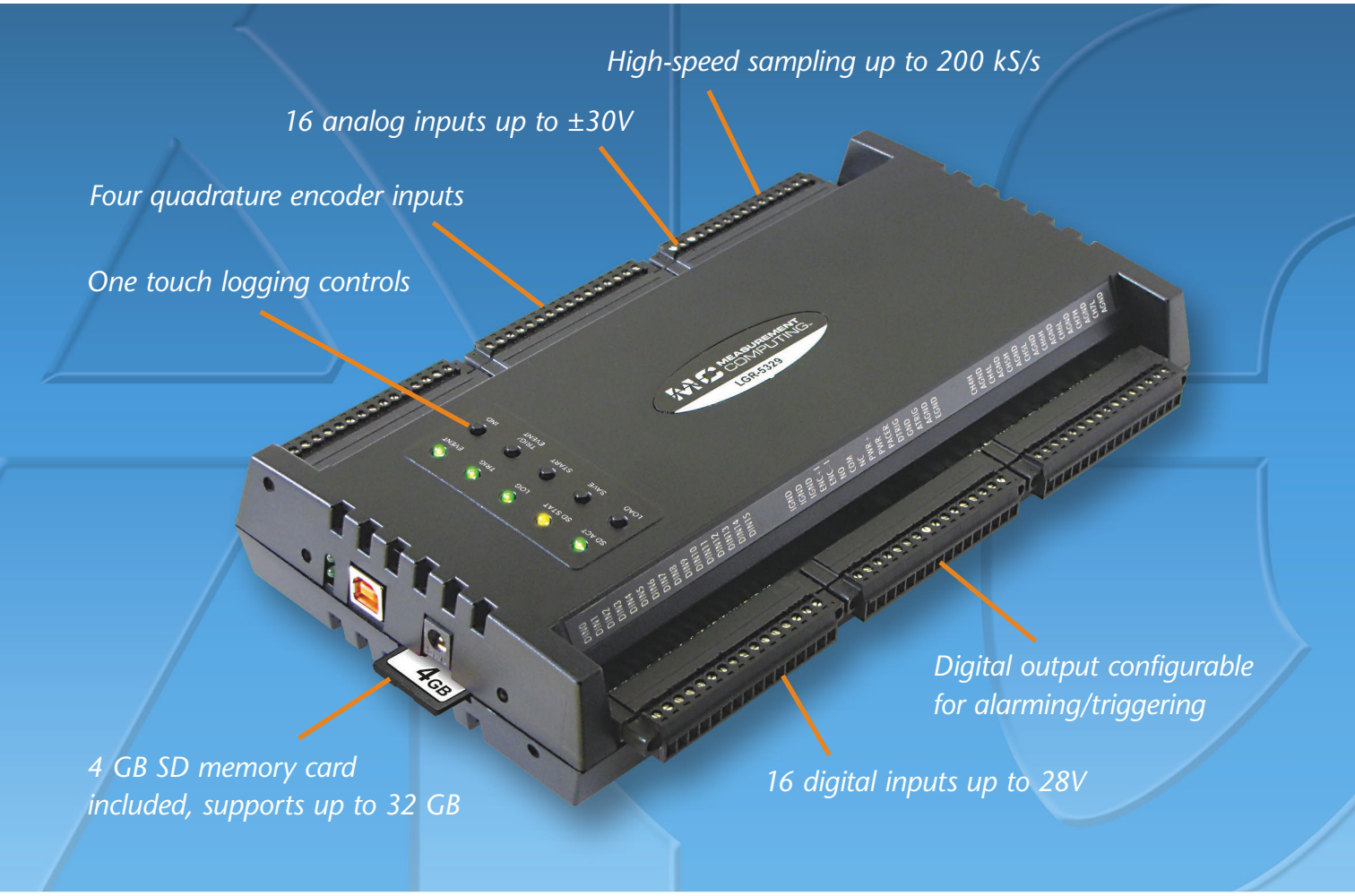

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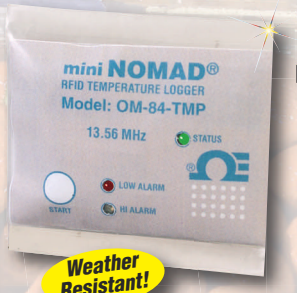

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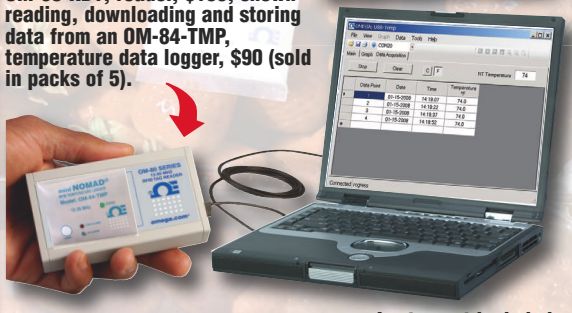

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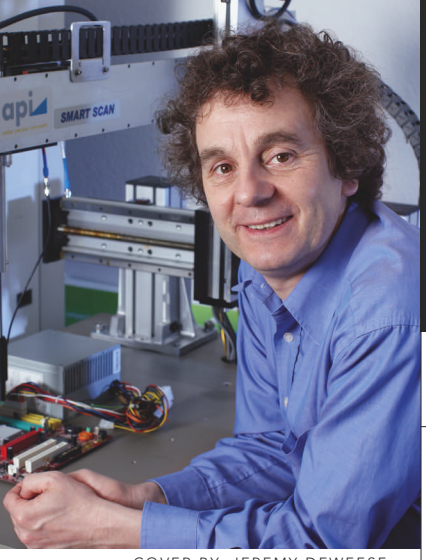

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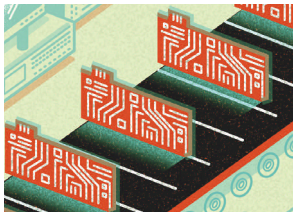

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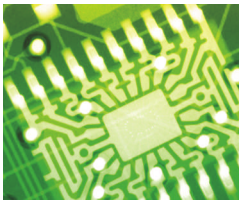

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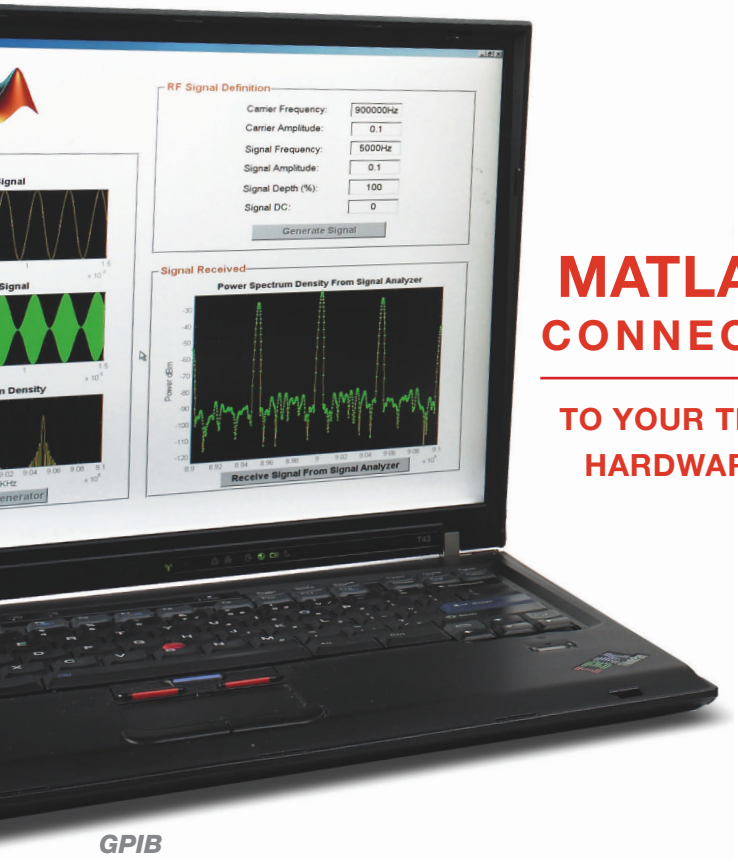

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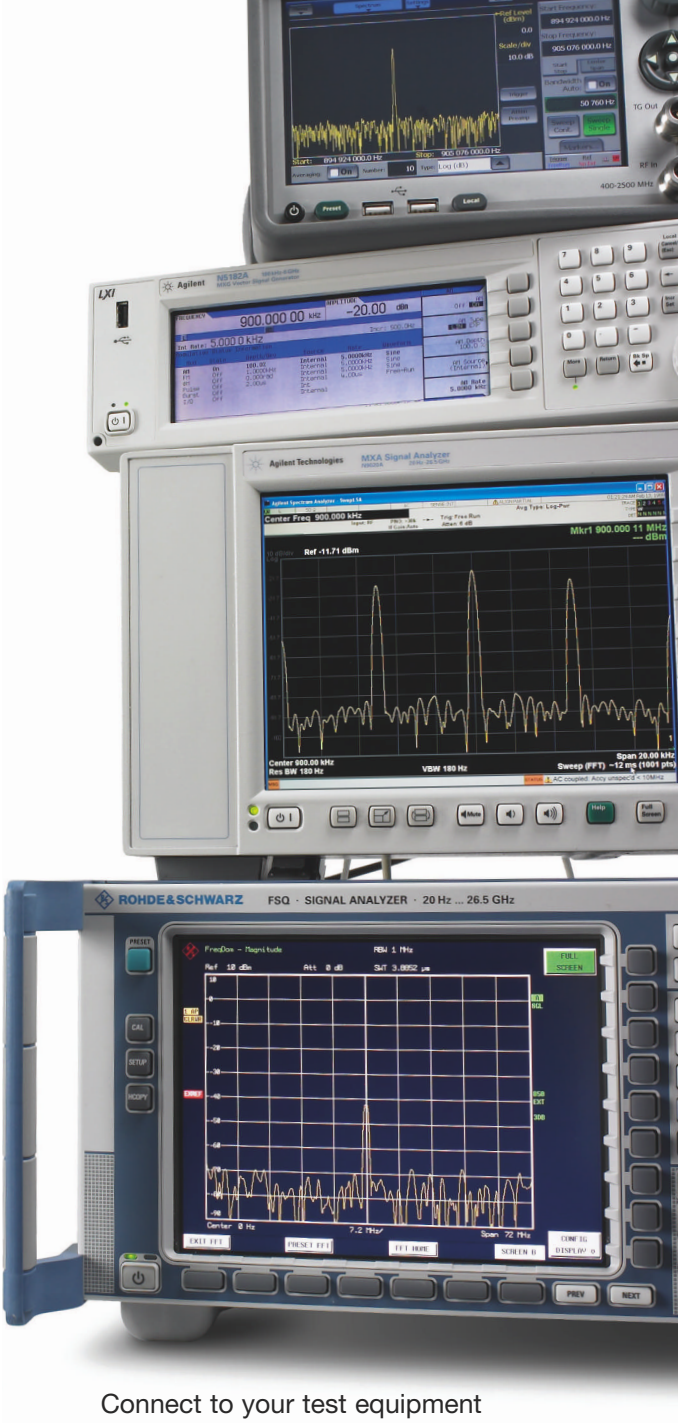

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Mixed-signal multisite test

In a two-part series on the *Test & Measurement World* Website, Jin-Soo Ko of Teradyne discusses the use of multisite testing for mixed-signal SOCs and SIPs. Part 1 discusses how the limited number of channels on AC instruments and limited DIB real estate restrict the number of sites that can be used for multisite testing of mixed-signal devices. Part 2 describes an approach he calls ACEX that expands mixed-signal multisite test capability.

www.tmworld.com/guest_multisite

Blog commentaries and links

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RICK NELSON
EDITOR IN CHIEF

Flight disruption lacks hard data

The amazing disruption to European air travel continues, with widespread repercussions. My colleague David Greenfield of *Design News* had expected to be attending Hannover Fair last month, but volcanic ash kept him stateside. (According to Hannover Messe, "Despite considerable obstacles in international aviation, HANNOVER MESSE 2010 will take place as scheduled. The fair opened on the evening of Sunday, April 18.") Closer to home here in Boston, many international runners were unable to get to the Boston Marathon.

The Iceland volcano could continue erupting for weeks or months, suggesting ongoing disruption. From an *EDN* and *Test & Measurement World* perspective, a variety of upcoming events could suffer the effects of air-travel delays: the International Microwave Symposium in Anaheim in May, the Design Automation Conference in Anaheim in June, and Semicon West in San Francisco in July. I'm also planning to attend IMEC's annual technology review in Leuven, Belgium, in June—my concern there would be getting to Belgium and being prevented from returning by another blast from Eyjafjallajökull, or an initial eruption from its neighbor.

There seems to be very little hard data available on the level of danger the volcanic ash presents.

Of course, apart from its affects on international conferences, the volcano could have drastic effects on daily life. As *Washington Post* columnist Ann Applebaum, who lives in Poland, wrote last month, "Already, the past several days have revealed that we rely on air travel for far more things than we usually imagine. Things such as supermarkets—all that fresh fruit—and florists. Things such as symphony performances, professional soccer matches and international relations. In fact, 'European integration,' as we have come to understand it, turns out to be utterly dependent on reliable air travel."

What's frustrating is that there seems to be very little hard data available on the level of danger the volcanic ash presents. No one is talking safe parts-per-million levels of ash particles, for example. The only effort at gathering data seems to be to operate test flights and look for damage afterward. That seems about as reliable as driving one Toyota on a test track, hoping to definitively reproduce an instance of sudden unattended acceleration. Lack of damage after one or a few test flights doesn't guarantee the ash poses no threat, just as successful low-speed operation of an automobile on a test track without observing sudden unattended acceleration doesn't mean the phenomenon doesn't exit.

Finding the proper course to take in the face of continuing or resuming eruption remains the challenge. The economic consequences are serious, with airlines losing money. And there are reports that the flight disruption is affecting the electronic supply chain, with automotive factories in China unable to obtain electronic components from Germany.

European transportation officials admit to uncertainty with regard to the models they use to predict the dispersion of the ash cloud and its potential impact on airplane engines. In the face of growing discontent from the airline industry, they are understandably erring on the side of safety. Let's hope the engineers and scientists can refine the models to get planes back in the air. T&MW

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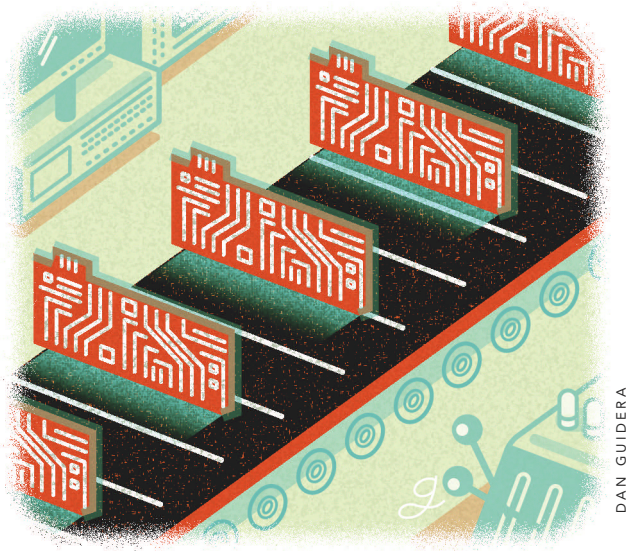


DAN GUIDERA

Tara Drennen is a test engineer with Express Manufacturing, a contract manufacturer with facilities in California and China. Drennen, who works in the company's Santa Ana, CA, office, is responsible for test-system integration, which involves specifying equipment, system troubleshooting, system upgrades, and test reviews. Senior technical editor Martin Rowe spoke with Drennen by telephone.

Q: What kinds of products do you manufacture, and how is the manufacturing divided between California and China?

A: Industrial controls and telecom boards are the bulk of our manufacturing, although we're moving into medical and military. High-volume products are manufactured in China, but we do a lot of manufacturing here. All military products are manufactured in California. We do all of the process engineering, manufacturing engineering, and test engineering here. Engineers in China build test systems per our instructions.

Q: How do you handle system integration?

A: Customers send us their test specifications and their product specifications. I evaluate the specs and determine what it will take to meet them. I report to the customer on the time required to test their products and the tradeoffs between manual, semiautomatic, and fully automated testing. The tradeoff is test time versus engineering costs.

I try to get the customer to let the tester do the measurements wherever possible, because that produces more repeatable results while minimizing human errors. We also make recommendations to PCB [printed-circuit board] designers on where to place components for testability and optimize the boards per panel for production and test efficiency.

Q: Do you specify entire test systems?

A: It varies. Some customers provide a test system for us to upgrade and program, although some will provide test code as well. Others have test procedures and perhaps test fixtures, but they don't supply the test system. We adapt our in-house ICT [in-circuit test] systems to perform ICT, but each product family requires a custom functional test fixture.

Q: Do you write test code?

A: We may write the code ourselves, often in Visual Basic, but some customers provide code written in LabView or Python that our programmers can integrate into our systems. For example, we used customer-supplied LabView code for a system that uses USB data-acquisition modules and RS-485 interfaces integrated into a test fixture. The DUT [device under test] uses an ARM-7 processor that contains eight serial buses. The data-acquisition modules simulate ADCs in the DUT. Using these kinds of instruments may eliminate using "golden" boards in many testers.

Q: When do you use golden boards?

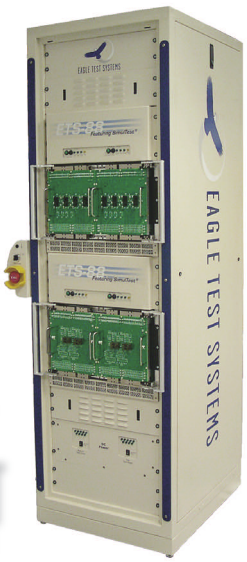
A: We often use a golden power board from a customer in a test system to properly apply power to a processor board under test. That way, we don't have to program test equipment to simulate power switching for a DUT.

Q: Do you analyze test results?

A: Yes, and we can recommend design changes based on test results. For example, we found one customer's boards had a tantalum capacitor that would often fail. The board was applying 18 V to a part rated at 25 V—that's too close for tantalums. Changing to a 50-V capacitor eliminated those failures. T&MW

Every other month, we publish an interview with an electronics engineer who has test, measurement, or inspection responsibilities. If you would like to participate in a future column, contact Martin Rowe at mrowe@tmworld.com. To read past "Test Voices" columns, go to www.tmworld.com/testvoices.

Teradyne ETS-88 is the 2010 Test Product of the Year



On April 6, the editorial staff of *Test & Measurement World* announced that the Teradyne ETS-88 multisite test system has been selected as the 2010 Test Product of the Year. The ETS-88, which won the 2010 Best in Test award in the Semiconductor Test category, received the most overall votes in the annual Best in Test balloting.

The Teradyne ETS-88 features a modular architecture coupled with a multithreaded operating system to provide configuration flexibility and optimized cost of test for power-management and catalog linear devices. The system, available with one to four test "quadrants," supports 32 to 128 digital pins and 72 to 288 analog pins. Quadrants can be used independently to test different devices on different peripherals; or quadrants can be linked for multisite testing with parallel test efficiencies approaching 100%, quadrant to quadrant. Alternatively, multiple quadrants can be used to realize true concurrent test.

We announced Teradyne's win during a ceremony held in Las Vegas, during which we also honored the winners of the annual Test Engineer of the Year award, Test of Time award, and Best in Test awards. Lisa Moder, the Test Engineer of the Year, was profiled in our April issue, where we also announced the winners of the Best in Test and Test of Time awards. www.tmworld.com/awards.

TEST PRODUCT OF THE YEAR

Presto and CEA-Leti to test 3-D devices

Presto Engineering and CEA-Leti, a French research and technology public organization, have begun a three-year collaboration to extend Presto's test, reliability, and failure-analysis products to the testing of TSVs (through-silicon vias), the interconnects between levels on 3-D devices. The two firms will work together in a common lab that will include Presto's new R&D center at CEA-Leti's facility in Grenoble, France.

"CEA-Leti has industry-leading expertise in 3-D integration, advanced interconnects, and TSVs, and by working side by side with CEA-Leti's experts, Presto will build on our proven product engineering capabilities for the arrival of TSVs," said Michel Villemain, CEO of Presto Engineering, in a prepared statement.

Through the collaboration, Presto and CEA-Leti will work to characterize the reliability, defect susceptibility, and electrical performance aspects of TSVs; identify existing test protocols that are appropriate for 3-D structures while developing new ones to meet new challenges; and bring up new diagnostic methods or tools to identify root cause of failures. The lab will make the ATE and debug process as well as the product engineering platform available for third parties. In addition to its broad goals, the joint lab will enable Presto to develop critical test and analysis techniques, such as probing specific areas of TSVs without affecting the device itself. www.presto-eng.com.

Editors' CHOICE

Agilent introduces 32-GHz oscilloscope

The race for the highest bandwidth oscilloscope has a new leader as Agilent Technologies has introduced the 90000-X series, which includes a 32-GHz model. The 32-GHz instrument (when running two of four channels), combined with its accompanying probes, forms a 30-GHz measuring system. Using a probe head with SMA connectors, you get a maximum bandwidth of 28 GHz.

Agilent achieves the high bandwidth through a multichip module designed to act like a Faraday cage around sensitive indium-phosphide analog components. Its 13.5-ps rise time, amplitude noise floor of 2 mV at 50 Mv/div, 32-GHz bandwidth, and jitter-measurement floor of 180 fs maximize signal fidelity. The instruments in the series don't use DSP techniques to boost bandwidth at the expense of noise.

The series consists of five DSOs (digital sampling oscilloscopes) and five DSAs (dynamic signal analyzers). The instruments start with a bandwidth of 16 GHz and cover 20 GHz, 25 GHz, 28 GHz, and 32 GHz on two channels, with all models operating at 16 GHz on four channels. All models sample at 80 Gsamples/s (two channels) and 40 Gsamples/s (four channels). Maximum waveform memory is 2 Gsamples/channel. Standard memory is 10 Msamples/channel.

Price range: from $131,000 for a 16-GHz DSO to $286,000 for a 32-GHz DSA. *Agilent Technologies, www.agilent.com.*

CALENDAR

Sensors Expo, June 7–9, Rosemont, IL. *Questex Media Group. www.sensorsexpo.com.*

Design Automation, June 13–18, Anaheim, CA. *ACM SIGDA and IEEE, www2.dac.com.*

Semicon West, July 13–15, San Francisco, CA. *SEMI, www.semiconwest.org.*

EMC Symposium, July 25–30, Ft. Lauderdale, FL. *IEEE, www.emc2010.org.*

Autotestcon, September 13–16, Orlando, FL. *IEEE, www.autotestcon.com*

To learn about other conferences, courses, and calls for papers, visit www.tmworld.com/events.

Netropy assesses WAN conditions

Editors' CHOICE

Apposite Technologies' Netropy network emulator simulates complex WAN topologies so engineers can benchmark, troubleshoot, and optimize enterprise applications, including those involving file sharing, network storage, and IP voice and video. The performance of applications operating over a WAN depends not only on the available bandwidth but also on the latency, jitter, loss, and network congestion. Netropy models dozens of concurrent WAN links at up to 10 Gbps.

Netropy allows engineers to simulate multisite networks by emulating simultaneous connections between centralized resources and remote offices, benchmark multiple products or conditions by running side-by-side comparisons, run multiple tests concurrently to slash test time, isolate applications to measure the impact of particular conditions on each one, and model advanced queuing and loss to build models of complex network conditions.

The Netropy family consists of the Netropy N60 (one 1-Gbps emulation engine with up to 15 WAN links), Netropy N80 (four separate 1-Gbps emulation engines of 15 WAN links each), and Netropy 10G (one 1-Gbps and two 10-Gbps emulation engines).

Base price: $8000. *Apposite Technologies, www.apposite-tech.com.*

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Bandwidth demand pushes optical communications

> > > OFC/NFOEC conference and exhibition, March 21–25, San Diego, CA, www.ofcnfoec.org.

At this year's OFC/NFOEC, it became clear that 40G/100G Ethernet is for real, and the economy is rebounding. Many people reported improving business because the demand for bandwidth keeps growing.

Alcatel-Lucent executive VP Philippe Keryer told an audience that 100G Ethernet will arrive in core networks this year. "This will be the year of coherent modulation," he said, "using the same infrastructure as today's 10G Ethernet."

Exfo demonstrated 100G (111-Gbps) transmissions using its optical modulation analyzer and an **Ixia** 40G/100G Ethernet tester. Exfo also exhibited its constellation analyzer and its optical sampling oscilloscopes.

Agilent Technologies introduced an optical modulation analyzer for 28/32-Gbaud transmitters and links. Agilent also introduced single-port and four-port tunable laser modules and two-channel and four-channel multimode attenuator modules for its 77-Series optical test instruments.

Yokogawa demonstrated the AQ1200 Multi Field Tester OTDR. The company's AQ7275 OTDR supports optical links from the home through the network core, and its AQ1300 10G Ethernet tester includes electrical and optical ports for 10-Mbps through 10-Gbps links.

Aragon Photonics exhibited its Bosa Phase optical complex spectrum analyzer that displays complex spectrums, complex fields, eye diagrams, and constellation diagrams. **Centallax** exhibited its 12.5-Gbps parallel-channel BER tester, its 40-Gbps BER tester, and its 10-Gbps BER testers, clock-recovery modules, and clock synthesizer.

Anritsu's MS9740A optical spectrum analyzer has a better than 58-dB dynamic range and –90-dBm minimum light-reception sensitivity. **Averna** demonstrated its Proligent data-analysis software used for optical tests. **JDSU** exhibited the ONT-506 40G/100G network physical-layer tester. **Tektronix** showed the DSA8200 digital phosphor oscilloscope series with optical modules. **Optametra** exhibited its 28-GHz coherent receiver connected to **LeCroy** and Tektronix oscilloscopes. The receiver lets you analyze QPSK signals with constellation diagrams and eye diagrams. **Picosecond Pulse Labs** exhibited its pattern generators and BER testers with LeCroy oscilloscopes.

Synthesys Research showed the BertScope with an increased speed of 26 Gbps for 100-Gbps links. The company's 25000A clock-recovery unit now runs at 28 GHz. **ILX Lightwave** exhibited is 7900B laser-diode test system. **Luna Technologies** showed its OVA 5000 optical vector network analyzer and its Optical Backscatter Reflectometer platform—a high-resolution OTDR with millimeter resolution that helps users find faults in optical fibers close to connectors.

The N7711A adds four laser sources to the 77-Series of optical testers.
Courtesy of Agilent Technologies.

Optical transducer manufacturer **Opnext** had several demos of 40G and 100G optical links. A 100GBase-LR4 demo used an Ixia 40G/100G Ethernet tester connected through 120 km of fiber to an Anritsu MS9710C optical spectrum analyzer. Another demo featured a 40G-LR4 link, which consisted of four 10-Gbps links running on four wavelengths in a single fiber. T&MW

Aldrin buzzes at MSC

> > > Measurement Science Conference, March 22–26, Pasadena, CA, www.msc-conf.com.

Former astronaut Buzz Aldrin spoke during the 2010 MSC luncheon about how measurements played an important role in the space program. He pointed out how reaching the moon was truly a joint effort among NASA; numerous companies; Congress; Presidents Kennedy, Johnson, and Nixon; and the American people.

Technical sessions covered issues such as RF and temperature measurements, measurement uncertainty, and metrology education. In the RF measurement session, Mike Ashcroft of Fluke discussed calibrating spectrum analyzers so they have minimal effect on measurements. He noted that you need to understand the harmonic distortion that a spectrum analyzer adds to a measurement, and he discussed how to test for distortion. He suggested that you set the mixer at around –30 dBm and look at relative amplitude. Then, change the input attenuation by 10 dB. If the distortion doesn't change, then the spectrum analyzer isn't contributing to the distortion.

Fluke exhibited a multifunction calibrator for handheld digital multimeters and analog meters. **Tegam** introduced an RF transfer standard that covers frequencies up to 26.5 GHz. Applications include automotive collision-avoidance systems and wireless HDMI.

Agilent Technologies exhibited several signal analyzers, including the PNA (N5242A), which is designed for noise-source calibration. **Spectracom** exhibited a line of microwave instruments it has acquired from Pendulum Instruments as well as its 8195B GPS master oscillator. **Guildline Instruments** demonstrated its 6623A-300 current source and the 6664 scanner for automating high-resistance measurements. T&MW

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RICK NELSON
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Interfacing North American OEMs and Asian CMs

Contract manufacturers can excel at building products, but they may not excel at testing them. That's the premise of Robin Tian, the CEO of SiFO Technology, who is positioning his firm, headquartered in Suzhou, China, to be the interface between North American OEMs and Asian CMs (contract manufacturers).

In an interview I conducted with Tian at last month's IPC APEX Expo in Las Vegas, he noted that OEMs have traditionally developed board-test processes to ensure their CMs are delivering quality products. Given travel-budget and other restrictions, however, the OEMs often lack the resources necessary to install, troubleshoot, monitor, and upgrade test programs and systems at their CMs' Asian facilities. To alleviate this problem, SiFO at APEX introduced its Independence test services program, under which the company's China-based engineers will develop test programs as well as in-circuit and functional test fixtures for CMs' use on behalf of North American OEM customers. In addition, Tian said, SiFO can also serve as a China-based third party that can monitor a CM's test processes.

CEO Robin Tian is positioning SiFO Technology as a test-services supplier who can work on behalf of North American OEMs at their Asian CMs.

Tian explained, "The Independence program is the direct result of SiFO's experience working with well-known OEMs in Silicon Valley, as well as [the result of] what my team and I learned while working for companies like Agilent and Teradyne to support OEMs and their contract manufacturers in China." More than a consulting firm, SiFO has 18,000 ft^2 of manufacturing space in Suzhou and an additional 10,000 ft^2 in Shenzen, where it can build fixtures and configure test systems. Tian said SiFO has already delivered 120 functional test systems and more than 2000 fixtures and programs purchased by US OEMs for use by their CMs in China.

Tian cited several examples of success. In one instance, a CM was experiencing damage to a networking board during in-circuit test—a problem the CM couldn't resolve and that the OEM lacked the resources to address. SiFO engineers located and solved the problem's root cause while adding boundary-scan test to improve test coverage. In another example, a CM was unable to meet volume test requirements after the launch of an electronic book reader. SiFO delivered four additional functional test systems within five weeks while reducing tester footprint and improving operator ergonomics.

In yet another example, an OEM determined it couldn't rely on its CM to procure functional test fixtures of sufficient quality to test its notebook computers. SiFO acquired an additional 8000 ft^2 of manufacturing capacity, purchased 12 CNC (computer numerical control) machines, and hired 30 operators and 10 engineers to deliver 70 fixtures per day.

Tian acknowledged that CMs might balk at working with SiFO as they would prefer to provide the services and systems themselves, but he added that ultimately the ability to deliver high-quality products is a win for the CM as well as for the OEM. T&MW

To read past "Tech Trends" columns, go to www.tmworld.com/techtrends.

Verigy ships V93000 Port Scale RF systems

Verigy reports it has shipped multiple V93000 Port Scale RF systems to a repeat customer for testing RF SOC devices used in low-cost handsets. "This customer currently has several V93000 Port Scale RF test systems being used to test RF SOC devices in production," said Pascal Ronde, VP of worldwide sales, service, and support at Verigy. "The flexible architecture of the platform enables users to increase their manufacturing throughput by testing not only radio receivers, but also other critical parts." www.verigy.com.

Teradyne debuts Test Expert for Spectrum v9.0

The latest version of the software for Teradyne's Spectrum test system includes Test Expert, a component of Siemens PLM Software's Tecnomatix productivity software. The integrated software, Test Expert for Spectrum v9.0, interacts with the Spectrum test-program development environment to expedite the importation of electronic CAD data, the selection of test-probe locations, and the automation of the test-fixture design. www.teradyne.com, siemens.com/plm.

Advantest introduces 3-D imaging analysis system

Advantest has commercialized the TAS7000 3-D imaging analysis system, which employs the company's terahertz wave technology to perform nondestructive scans of sample materials and deliver 3-D visualization of results. The system is initially being marketed to the automotive and heavy-equipment industries, where it can be used to evaluate particulate matter in emissions from diesel engines. www.advantest.com.

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ANN R. THRYFT
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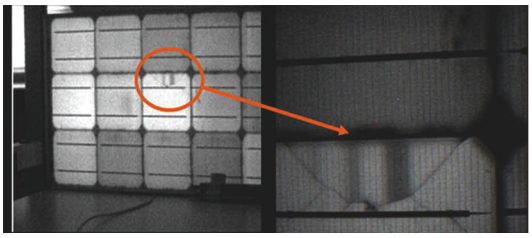
Short-wave infrared looks at solar wafers

The drive to increase both production efficiency and product efficiency of crystalline-silicon PV (photovoltaic) wafers and cells is leading manufacturers to explore a number of different inspection techniques. Engineers are using SWIR (short-wave infrared) technology, primarily in design or failure-analysis labs, to check PV wafers for voids and cracks, as well as checking cells and panels for short circuits and incomplete current conduction, which can decrease efficiency or lead to the failure of an entire panel.

"Manufacturers of solar wafers and cells use other techniques to perform these checks, and they work pretty well to sort good from bad," said Doug Malchow, business development manager for industrial products for Sensors Unlimited Goodrich ISR Systems. "This past year, we've seen more interest in improving solar-cell efficiencies, and therefore more interest in the use of our SWIR technology and two imaging techniques, photoluminescence and electroluminescence, to find out why performance is bad."



SWIR technology combined with electroluminescence imaging techniques reveals defective areas in the solar cells (right, close-up) of a commercial solar cell panel (left). Courtesy of Goodrich.

Although light in the SWIR band of the spectrum is invisible to the human eye, it casts shadows and creates contrast in images created with linescan and array cameras based on InGaAs sensors, said Malchow. These sensors are extremely sensitive and can detect discontinuities in conditions with extremely low visible light.

At SWIR wavelengths, silicon becomes transparent. Since circuits are created on a wafer's front side, InGaAs sensors can create images of these circuit patterns on crystalline-silicon PV wafers and standard silicon wafers through their back sides, to determine whether they are aligned properly and to find cracks and voids, said Malchow. "When finished crystalline PV solar cells are connected to a power supply and voltage is forced into them, it creates an electroluminescent glow that can be imaged to find cracks, dead spots, contaminants, and weak areas," he said.

The glow's intensity indicates the amount of collection efficiency in each cell and each panel. When a panel contains a mix of cells of different efficiencies, the more efficient cells waste huge amounts of energy pumping current through the less efficient or dead cells, bringing down overall panel output and efficiency.

"Cell manufacturers want to identify problems long before they put the electrodes on the cell," he continued. "Imaging photoluminescence from cells or even unprocessed wafers permits catching major material or processing problems before building expensive inventory that ends up being scrapped."

InGaAs linescan or area cameras can be used in conjunction with an IR microscope to inspect very fine detail in surface or buried layers of standard silicon wafers, said Malchow, as well as to give a rough measure of layer thicknesses. For those who need to inspect wafers at very high speeds, the new Goodrich SU1024LDH2 linescan camera will reach line rates of over 91,000 lines/s, reducing exposure times. "Our cameras are also used for examining structures inside MEMS devices, to ensure that nothing is left from the process to obstruct movement," he said. T&MW

To read past "Tech Trends" columns, go to www.tmworld.com/techtrends.

Multispectral camera gains GigE Vision

JAI has added two GigE Vision interfaces to its multispectral, two-CCD camera that simultaneously images visible and near-infrared light spectra through one lens. The new model AD-080GE incorporates two ⅓-in., 1024x768 resolution, progressive-scan sensors, bonded to a customized optical prism that splits light into visible and NIR channels. The camera's frame rate in continuous operation is 30 fps. www.jai.com.

Driver package adds language support

Release 2.2 of Basler Vision Technologies' Pylon camera driver package adds support for C and C# and Microsoft's .NET, Visual Basic 6.0, and VB.NET programming languages. The release also provides a GenICam-compliant API (application programming interface) for configuring Camera Link cameras. The 2.2 package and software development kit can be downloaded for no charge from the company's Web site. www.baslerweb.com.

Smart-camera software is Windows 7 compatible

PPT Vision's 9.0 release of its Impact smart-camera vision software suite is compatible with Microsoft Windows 7. Other changes include the addition of an OPC (OLE for Process Control) server for a supplemental communications link with plant process-control systems and reorganized toolboxes for a more intuitive layout. www.pptvision.com.

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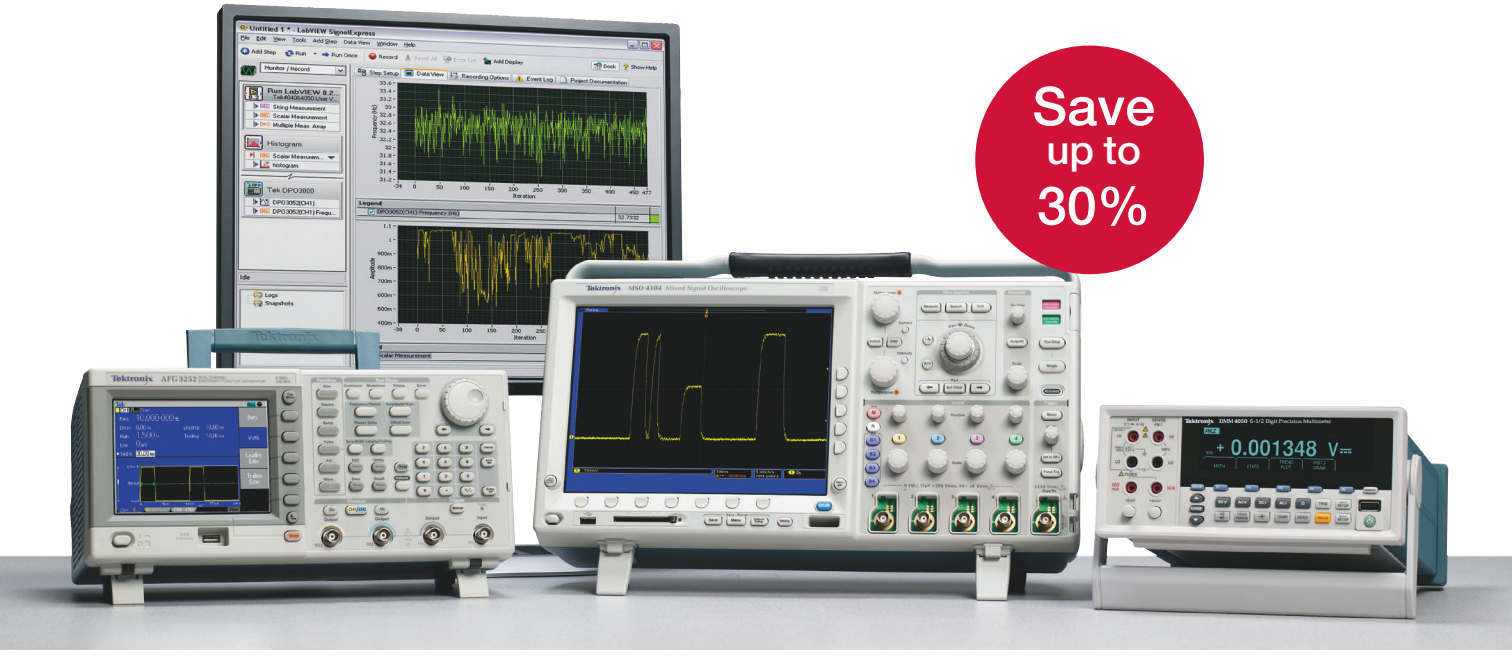

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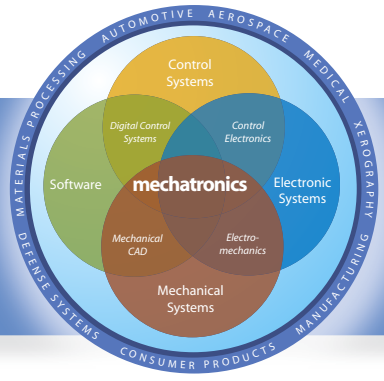


Friction fundamentals and accelerating cars

In elections it's always the economy; in engineering it's the fundamentals

Friction may well be nature's most useful phenomenon. Without it, walking would be impossible and there would be no belt drives, no clutches, no wheels, and no brakes. In machinery in which it is not the driving force, however, friction is an undesirable parasitic effect, generating heat, causing wear, and wasting energy. So, whether the goal is to reduce friction or enhance it, the proper combination of geometry, materials, and lubrication must be employed in a design—a proper tribological approach. Tribology is the study of friction and wear. It has been estimated that the correct application of tribology throughout US industry could save the country $500 billion annually.

Much has been written about the problems with uncontrolled acceleration of automobiles due to faulty accelerator pedals. Friction has been identified as the likely culprit, and the proper combination of geometry, materials, and lubrication will likely lead to a solution. Why did this happen? It is too early to answer that question with any certainty, but I do know that most engineers, including mechanical engineers, do not fully understand the friction phenomenon. Failure to understand the fundamentals of such a pervasive physical effect is bound to lead to design failures, some of which might be catastrophic.

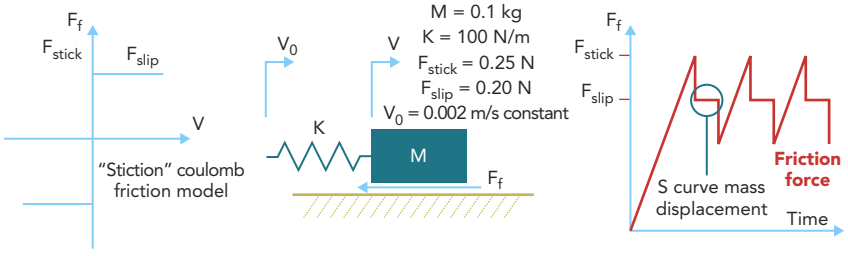
Stick-slip motion is a common behavior associated with friction. In a typical stick-slip experiment, one end of a spring is attached to a block sitting on an unlubricated horizontal surface. The other end is moved horizontally with a constant velocity. How will the block move? It depends on the physical system parameters, but one possible outcome is stick-slip motion, as shown in the **figure.** When the spring force exceeds F_{stick}, the mass accelerates, the spring elongates, and the mass comes to rest. The process then repeats, creating the stick-slip behavior. A model used to describe the friction phenomenon must be able to show this behavior. The automobile accelerator pedal relies on a balance between the return-spring force and sliding friction, which could vary over time due to wear and contamination, to perform effectively and safely.

In the automobile electronic accelerator pedal assembly—it's electronic, because when the gas pedal is depressed, a sensor tells the car to accelerate—a certain amount of friction makes it easier for the driver to maintain a steady throttle setting and also reduces fatigue from pushing against the pedal return spring continuously. The designed-in friction is meant to simulate the intrinsic friction that is present in a traditional throttle cable as it passes through the cable housing. If the friction is excessive, the pedal return spring cannot return the pedal when the driver's foot is removed, and the pedal sticks in the partially open position.

Changing the friction characteristics will change the accelerator feel for the driver. In addition, if wear or contamination is allowed to occur and change the friction characteristics, not only will the pedal feel change, but the safe operation may also change. The original problem and proposed solution for Toyota can be viewed at designnews.hotims.com/27742-516.

The Toyota pedal assembly includes a shoe that rubs against an adjoining surface during normal operation. Due to the materials used, wear, and environmental conditions, these surfaces may, over time, begin to stick and slip instead of operating smoothly. In some cases, friction could increase to a point that the pedal is slow to return to the idle position or stick, leaving the throttle partially open. A solution is to insert a spacer that will reduce the friction between the friction shoe and the adjoining surface, thus eliminating the excess friction that can cause the pedal to stick.

In a mechanical design, a proper tribological approach must be taken to ensure safety, performance, and energy-efficient operation. T&MW



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Robert C. Greenheck Chair in Engineering Design & Professor of Mechanical Engineering, College of Engineering, Marquette University.

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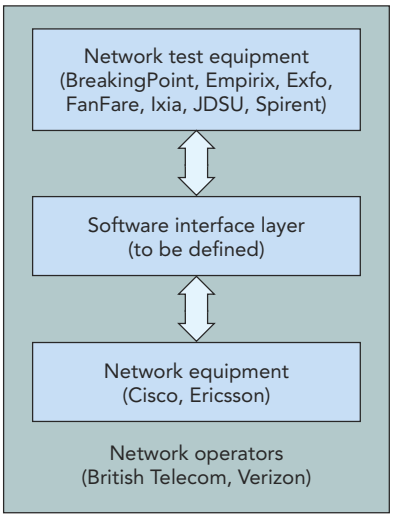
COMMUNICATIONS TEST

Forum to define network test interface

On March 16, the Network Test Automation Forum (NTAF) was launched by companies in the networking and communications industries. The forum consists of several network test-equipment makers, network equipment manufacturers, and two service providers. According to a press release, "The forum asks test equipment vendors to collaborate with their customers to define an open and advanced automation framework."

What does that mean? To find out, I met with Vikas Arora, CTO of Exfo, on March 23, during this year's OFC/NFOEC conference in San Diego. Arora explained that the goal of the forum is to develop a software layer that resides between network equipment such as switches and routers and network test equipment. The software layer should know what's on the network and provide a communications interface. The idea is to minimize integration of network and test equipment and provide a common communications platform rather than a set of proprietary interfaces. The **figure** shows the layer between test equipment and network equipment.



A software layer between network elements and test equipment forms a common application programming interface.

The concept is similar to that of VISA (virtual instrument software architecture), which was developed in the early 1990s. VISA provides a common API (application programming interface) between instrument drivers and low-level devices drivers. A user simply defines the communications bus for each instrument (GPIB, VXI, PXI, serial, USB, or Ethernet), and the instrument driver sends read, write, and other commands to VISA. Test-equipment makers have their own version of VISA, but the API is common to all. In the case of NTAF, the communications bus that connects test and network equipment will be Ethernet.

Martin Rowe, Senior Technical Editor

INSTRUMENTATION

Transparent clock improves network timing

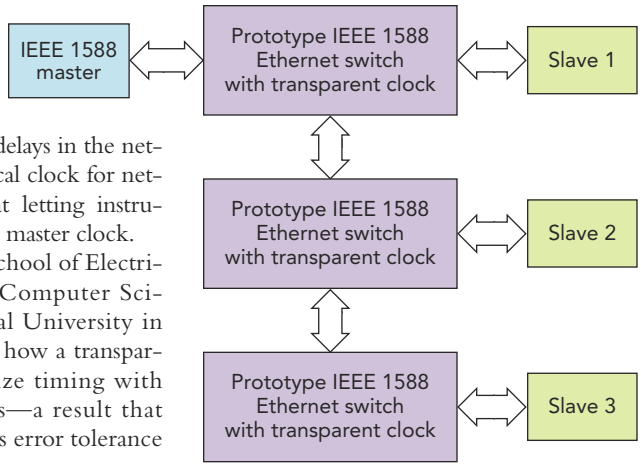
When Ethernet-based measurement systems call for precise timing, you can use instruments and network switches that comply with the IEEE 1588-2008 Precision Time Protocol to synchronize clocks (Ref 1). To get the most out of IEEE 1588 in an instrumentation network, you need Ethernet switches that support the standard. These switches use a transparent clock that minimizes latency and delays in the network by providing a local clock for network nodes rather that letting instruments rely on the IEEE master clock.

Researchers at the School of Electrical Engineering and Computer Science at Seoul National University in Korea set out to prove how a transparent clock can minimize timing with errors as low as 30 ns—a result that goes beyond the 100-ns error tolerance specified in IEEE 1588. Their paper is available from a link in the online version of this article (Ref. 2).

The IEEE 1588 master clock and Ethernet switches use an FPGA (field-programmable gate array) developed by the researchers to implement the transparent clock. The researchers compared the timing errors between identical network configurations using switches with and without the transparent clock. Using a four-channel oscilloscope, the researchers found maximum errors of about 30 ns with the transparent clock (**figure**).

When using standard Ethernet switches, errors increased by 1000X to 30 µs for slave 3. The network used Gigabit Ethernet running at 50% capacity. Without traffic, timing errors for slave 3 were about 500 ns.

The FPGA consists of the Ethernet switch fabric, transmitter, receiver, clock, and MAC (media access control). A GMII (gigabit media-independent interface) connects the functional blocks to a



Transparent clocks transfer IEEE 1588 timing information from a master to slaves.

PHY (physical-layer interface) IC. The paper's authors report that the network latency varies depending on the PHY manufacturer, which adds a few cycles of timing uncertainty to the measurements.

IEEE 1588 is closely aligned with the LXI Standard, which requires that all Class A and B instruments conform with the timing protocol. But a network need not be based on LXI to reap the benefits IEEE 1588 offers.

Martin Rowe, Senior Technical Editor

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2. Han, Jiho, and Deog-Kyoon Jeong, "A Practical Implementation of IEEE 1588-2008 Transparent Clock for Distributed Measurement and Control Systems," *IEEE Transactions on Instrumentation and Measurement*, IEEE, Piscataway, NJ, February 2010. p. 433.

Comprehensive automated subassembly testing

USB data-acquisition modules stimulate, measure, and control RF amplifiers.

Doug Parrish, Comtech PST, Melville, NY

Functional testing often requires you to simulate analog and digital signals that a UUT (unit under test) encounters in actual operation. You also may need to emulate control signals and commands. I recently developed a system that tests four digital control board subassemblies used in RF amplifiers. Twelve USB data-acquisition modules built into a test fixture provide the necessary stimulus signals and measurements.

The subassemblies the system tests are two digital automatic loop-control boards that control the power output of the RF amplifier, one power amplifier logic board used for controlling and interfacing between the internal components and subassemblies of the RF amplifier and the internal motherboard, and one motherboard that is the primary interface board for communicating with our customer's interfaces that use Ethernet/LAN, RS-485, and RS-232 protocols.

The I/O signal types consist of TTL signals used as single-ended bits as well as 8-bit bytes that simulate discrete control and communication between subassemblies. The test system needs single-ended and differential-input analog channels to measure distributed power-supply voltages and RF detector outputs.

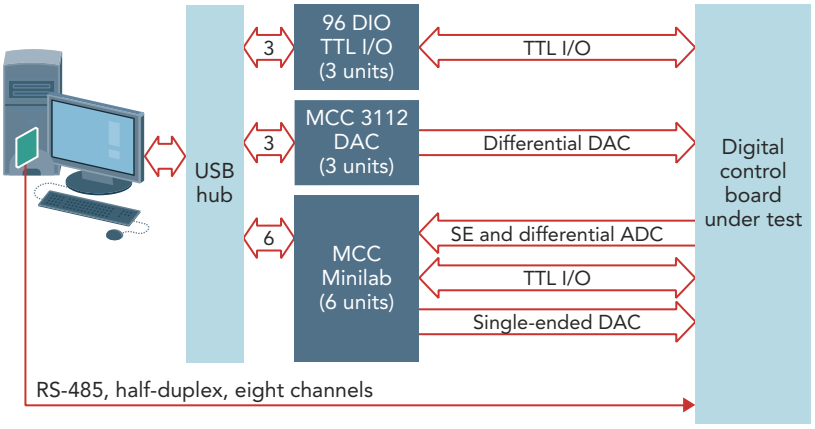
The tester also must create single-ended and differential analog voltages to dynamically simulate RF detector signals for the controller boards. Because the RF amplifier operates under software control, the tester has Ethernet, RS-485, and RS-232 ports for communicating with its motherboard.

The test system uses three different types of USB data-acquisition modules from Measurement Computing (MCC). The modules mount inside the test fixture, which provides portability among the test stations. That lets us change PCs without having to remove and reinstall PC plug-in cards.

Three MCC USB-DIO96H modules provide the TTL I/O signals. Although you can assign each 8-bit port to be an input or an output port, we needed two of the 96-channel digital I/O modules configured as outputs and a third configured as an input device. To test the TTL I/O signals of the digital-control boards, one DIO module stimulates the UUT's TTL inputs and the other two monitor the UUT's outputs.

Three MCC USB-3112 DACs satisfy the requirement for differential analog signals. To stimulate the differential analog inputs of the UUT, we drive the DACs in pairs. The test system also uses an RS-485 half-duplex interface to query the UUT for the magnitude of the differential analog input signal. This process repeats over a 0-V to 5-V dynamic range in 1-V increments. These signals simulate the analog voltage from RF detectors that logarithmically represent the output power level of an RF amplifier. Software compares the magnitude of the UUT's incoming analog signal against pass/fail criteria and then stores the results in Excel.

Six MCC USB MiniLab multifunction modules provide 30 single-ended analog inputs, one differential analog input, eight single-ended analog outputs, and digital I/O. The single-ended analog outputs simulate current or voltage metering from an external power supply. Differential analog signals control proprietary RF subassemblies over a 0-V to 1-V dynamic range. Differential signals maximize noise rejection.



A USB hub in the test fixture connects 12 instruments to a board under test.

The NI RS-485 half-duplex interface sends commands to the UUT, telling it to drive its analog outputs across various dynamic ranges. At the same time, the single-ended and differential ADC inputs measure the UUT's analog outputs. The results of a comparison to pass/fail criteria are stored in Excel.

All of the USB data-acquisition modules mount inside a 5¼-in. rack-mountable chassis. A self-powered USB hub provides a single-point USB connection to a PC. The UUTs mount on standoffs atop the cover of the chassis. All signals from the USB modules connect to the UUT through standard mating connectors in a wire harness (**Figure 1**). The online version of this article contains a link to a schematic of the test system (www.tmworld.com/2010_05).

The test software, written in Agilent Vee 7.5, lets the system test from one to four subassemblies. The operator can

choose between testing each subassembly in its entirety or simply testing all signals relative to a specific connector or connectors. The test software automatically programs the UUT's programmable logic devices—FPGAs, microcontrollers, and DSP controllers.

Once the testing begins, the operator can see the test results and pass/fail status for each signal, connector, and subassembly. The overall test time of each subassembly is approximately 5 min. For troubleshooting purposes, the operator can use a manual panel to stimulate and observe the response of a particular signal or pin. Operators can see test data on the PC monitor in real time while the system writes test data to Excel. We store the test data on the local PC's hard drive. When testing is complete, the system copies the data to a remote server for redundant and permanent data storage. T&MW

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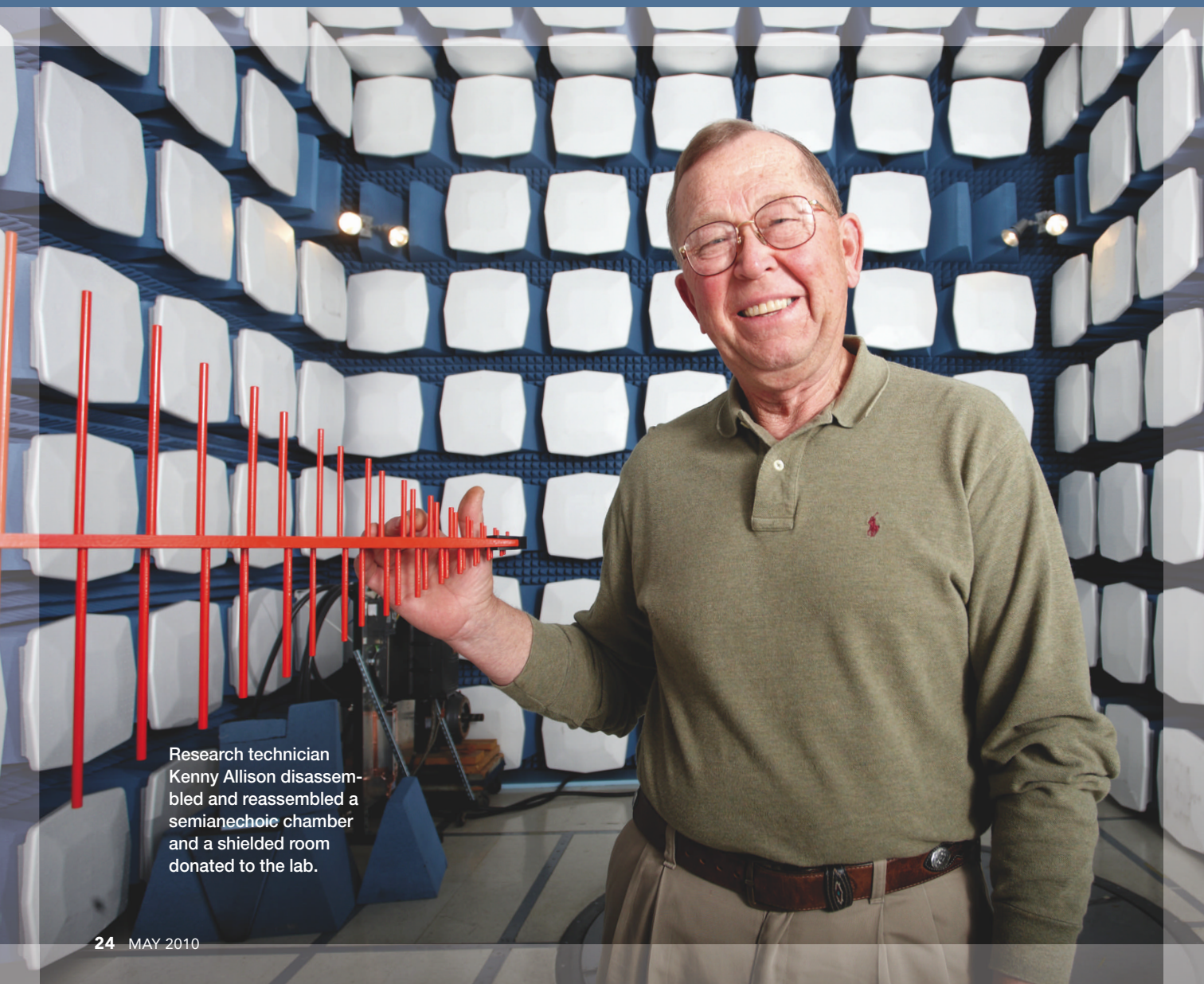
THE FACULTY AT THE MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY PROVIDES THE ELECTRONICS INDUSTRY WITH ENGINEERS WELL-EDUCATED IN EMC.

BY MARTIN ROWE, SENIOR TECHNICAL EDITOR

The EMC



Research technician Kenny Allison disassembled and reassembled a semianechoic chamber and a shielded room donated to the lab.

Giorgi Muchaidze, a former student at Missouri S&T, performs an ESD immunity test on a cellphone.

CONTINUUM

ROLLA, MO—EMC is one of those engineering disciplines that require a great deal of practical insight, which is why many EMC engineers have spent decades in the field. But those engineers will eventually retire. A new crop of engineers well-versed in EMC will need to step in.

That's where EMC labs such as the one at the Missouri University of Science and Technology (Missouri S&T) and other universities play an important role. In this college town about 100 miles from St. Louis, the lab's faculty is training future EMC engineers to understand why EMC problems occur and how to mitigate them.

The Missouri S&T EMC lab has six faculty members and about 25 graduate students who work closely with industry. Some of the companies working with the EMC lab through its EMC Consortium have included Altera, IBM, Cisco, Apple, Sony, Samsung, Freescale Semiconductor, NVIDIA, and LG. Recently, the EMC lab has started the Center for Electromagnetic Compatibility (Ref. 1), an Industry & University Cooperative Research Program funded in part through the National Science Foundation (Ref. 2). Three other universities—Clemson University, the University of Houston, and the University of Oklahoma—are also part of the Center.

Graduate students and faculty at Missouri S&T, which until January 2008 was known as the University of Missouri–Rolla, work closely with industry through the lab's EMC Consortium. Companies pay $60,000 a year for membership, which subsidizes students and faculty who investigate EMC problems, often to a fundamental level. "Industry engineers often need to find fast, effective, and inexpensive solutions to specific EMC problems and don't have the time to fully explore the fundamental causes of the problem," said Professor Richard DuBroff.

The knowledge gained through research is often incorporated into EMC software tools. "Consortium members are interested in how we develop software tools to help them in designs," said DuBroff. "We develop diagnostic techniques and theories on how circuits interact. Companies in the Consortium

PHOTOS: JEREMY DEWEESE

come to us to get a better understanding of EMI [electromagnetic interference] and how to prevent the problem from recurring. We sometimes can't get into the details of a design, but we try to understand why an EMC fix might work."

Associate professor David Pommerenke emphasized that "We try to study the most difficult EMC problems such as intrasystem coupling. In cellphones, for example, we've seen RF signals interfere with audio."

Pommerenke advises students on numerous other projects, many of which revolve around ESD (electrostatic discharge) and radiated immunity. "We try to understand and make projections through models for circuit behavior," he said. "We look for coupling paths and try to learn where current flows."

Under Pommerenke's direction, MSEE candidate Argha Nandy studied how ESD can travel through a flat flexible cable and couple into a circuit. Nandy developed a test set (**Figure 1**) consisting of two PCBs (printed-circuit boards). One board lets him inject an ESD pulse whose current travels through a flexible circuit to a second board that contains a D flip-flop IC. Nandy has two versions of the test board. One contains a typical TTL flip-flop, while the other contains a high-speed (8-GHz) device.

To characterize the flex cable, Nandy injected pulses into the blank board (left side of Figure 1). Using an oscilloscope, he measured how the pulse propagated through the flexible circuit to the flip-flop, looking for pulses on the flip-flop's clock line that would cause the device to change state. He also developed a full-wave model of the circuit in both the time domain and frequency domain. **Figure 2** compares the measured and predicted voltage at the flip-flop's clock input. The peak is enough to produce a change of state in the flip-flop.

Nandy and Pommerenke presented their findings at an EMC Consortium meeting in 2009. You can download a copy of their presentation, "Numerical prediction of ESD upset level," from a link in the online version of this article (www.tmworld.com/2010_05).

Associate professor David Pommerenke stresses that students apply a systematic approach to solving EMC problems.

JEREMY DEWEESE

Pommerenke teaches students to use a systematic approach to locating sources and resonances in circuits. "Suppose that noise in a laptop's memory couples into another part of the system. We want to understand the coupling paths. We run EMI scans on a product to find how electric and magnetic fields radiate in a circuit." Using mathematical processing of scan results, students find the coupling paths.

"We are developing software in Matlab to do the analysis," noted Pommerenke. "When we're satisfied with the models, we'll implement them in C++."

Software tools predict EMC behavior

Pommerenke's students aren't alone in developing software tools. Associate professor Daryl Beetner spends much of his time working with students to develop computer models of circuits that Consortium members use to predict EMC behavior. Beetner, who is a professor of computer engineering, works with a Consortium member company to model how ICs respond to EFT (electrical fast transient) events. His current goal: Develop a model of how energy couples into ICs so the company can design parts with greater immunity.

To develop the models, Beetner and PhD student Ji Zhang try to acquire as much information about an IC as possible. In some cases, IC manufacturers will provide equivalent circuits, but rarely will they provide complete schematics of an IC's protection circuits.

In addition to learning about ICs, students learn how energy gets into the devices. For example, current could enter an IC directly through an I/O line. Electromagnetic fields caused by interfering signals can also couple to I/O lines, producing unwanted current. Students run tests by firing an EFT generator into traces connected to the IC and tracking how current travels through a circuit.

Beetner and Zhang are currently measuring and modeling the I/O circuits in a microcontroller, and they plan to publish their results in a paper at the 2010 IEEE EMC Symposium in July (Ref. 3). **Figure 3** shows the test setup they use to measure the microcontroller's V-I characteristics at any two pins. An Agilent Technologies function generator creates the test signals, and an Agilent oscilloscope measures the response. One oscilloscope probe measures the voltage across the IC pins; the other measures the voltage across the 47-Ω resistor to find the input current. "We know there's some kind of diode structure in the microcontroller," said Beetner. "We look for breakdown voltage, parasitic resistance, and threshold voltage to build our models."

From the measurements, Beetner and his students developed a model of the IC that's far simpler than the actual device because of the difficulty in modeling active components. They also developed a model for a test board. Using the models, they apply a simulated EFT signal to the board and then predict performance of a powered device. "We have a good SPICE model of the IC that we want to use to

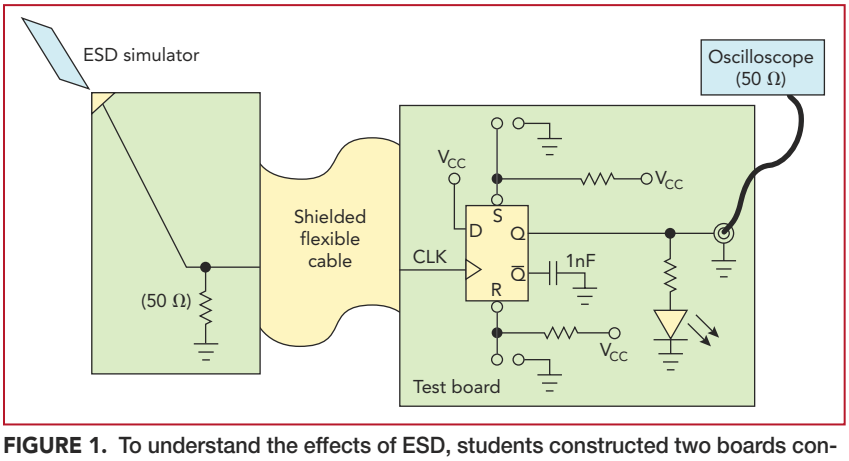


FIGURE 1. To understand the effects of ESD, students constructed two boards connected by a shielded ribbon cable. The second flip-flop on the chip is not used.

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34411A/ L4411A	6 ½	0.0030%	50,000 / sec	2.6 ms	GPIB, USB, LAN (LXI)
34420A	7 ½	0.0030%	250 / sec	.02 sec	GPIB, RS-232
3458A	8 ½	0.0008%	100,000 / sec	3.0 ms	GPIB

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predict the IC's susceptibility to electromagnetic fields produced by an ESD gun," Beetner said. IC designers can now use that model as a design tool.

Assistant professor Jun Fan has also been involved in the development of software tools that model circuits for signal integrity and intrasystem interference. A former EMC laboratory student, Fan worked in industry after completing his PhD and before joining the EMC lab faculty. He and his students study signal integrity to look for degradation of desired signals that can lead to false triggering in a digital circuit. Very often, a degradation in signal integrity is associated with some parasitic electromagnetic effects, similar to those effects associated with EMI.

Fan has updated the university's course on signal integrity and has continued the development of existing courses in computational electromagnetics. The signal integrity course is available on videotape and online though Missouri S&T's continuing-education program.

Fan is currently investigating how to use acoustic mechanical vibration as a means of detecting EMI at frequencies much higher than audio. "We're looking for traces of interfering electrical sources in other parts of a system that manifest as localized vibrations. For example, we might modulate an RF system's digital circuits with a 2.4-GHz signal and look for traces in the RF section."

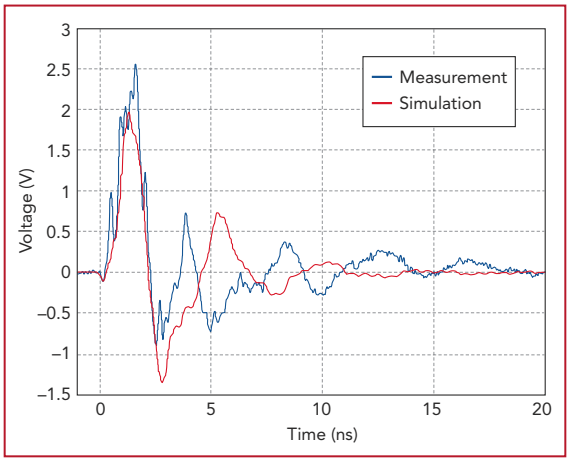

FIGURE 2. Oscilloscope measurements show how well the flexible circuit behaves compared to its simulation.

Finding solutions to EMC problems often requires an understanding of the materials used in electronic products. Research associate professor Marina Koledintseva studies how a material's composition and geometry affect its ability to absorb unwanted signals. From her research, she can develop mathematical models of a material's frequency behavior.

Koledintseva currently works with eight students on four projects. Working with equipment-maker John Deere, her students are investigating how to design ferrite chokes for use in automotive applications. Common-mode currents in cables can cause interference with circuits and systems, and Koledintseva's stu-

dents look to mitigate common-mode currents with ferrite chokes.

Koledintseva is also working with Cisco to characterize PCB dielectric materials, research that is important for signal integrity and high-speed digital design. The roughness of a PCB trace's surface can lead to signal loss in transmission lines, and this loss will affect the quality of the extracted dielectric parameters. This lack of accuracy becomes a problem as frequencies exceed 1 GHz. Koledintseva said, "We developed a method called DERM [differential extrapolation-redistribution method] that lets us separate the loss of conductors and dielectric materials on PCBs that takes into account the roughness of conducting surfaces in our analysis."

Custom probes simplify calculations

Measurements that students make to find coupling paths often require custom probes. DuBroff and Pommerenke advise students in the design and construction of near-field probes.

"Near-field probes can give a good representation of a field without too much mathematical processing," said DuBroff, whose background is in antenna theory. Probes respond to the angle of incidence of a field to a probe and to the field's activity. The probe will average the field over its loop area.

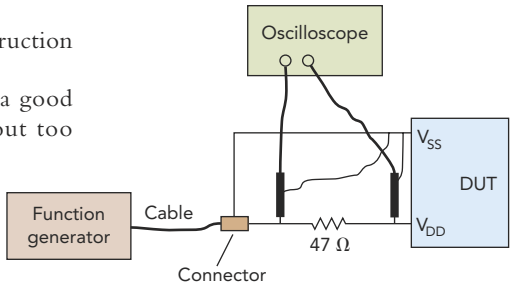

FIGURE 3. Students use an oscilloscope to measure the V-I characteristics of an IC's pins.

Electric fields, however, can affect a probe pointing in any direction. They can couple on the metal part of the probe and induce currents. Thus, electromagnetic fields aren't completely decoupled from a circuit. To compensate for that, Dubroff and others developed a process that involves measuring a known source with a probe in different orientations and then trying to characterize the probe's response. From that response, students can use software to compensate for deficiencies in the probe.

There's a tradeoff between a probe's size and its sensitivity. Because a loop probe responds to the time-changing magnetic fields that pass through the loop, the smaller the probe, the finer the resolution. Finer resolution makes isolating an emissions source easier, but it also makes the probe less sensitive. Pommerenke is pushing the limits of probe manufacturing by working with students to develop a probe that will measure the current in a single ball of a BGA (ball-grid array) IC package. *(continued)*

Missouri S&T students and faculty also use field probes to induce voltages and currents into devices as they research device failures. They often mount the probes on a scanner from Amber Precision Instruments (which leased space in the same building as the EMC lab) and look for emissions or inject interference into a board under test (**Figure 4**). Giorgi Muchaidze, a senior engineer at Amber and a former student at Missouri S&T, contributed to the scanner's design and uses it to create maps of PCBs or ICs that show the sensitive areas. He uses a TLP (transmission line pulser) in the scanner to produce pulses with controlled rise times of around 200 ps. (The TLP produces pulses with more controlled shapes than an ESD simulator.) The electromagnetic field that a pulse generates can couple into PCB traces and produce current in the circuit. "We look for functional failures," he said. "We want to see how the current flows in the EUT [equipment under test]."

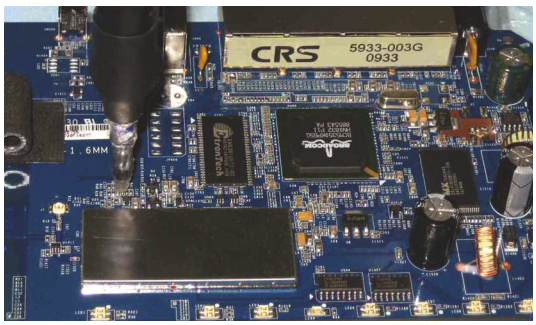

FIGURE 4. An EMI scanner moves probes over a PCB to measure current in the board or to inject current.

The scanner uses probes developed at Missouri S&T. Muchaidze demonstrated a magnetic-field probe that has a 5-mm x 5-mm loop. He uses the probe to inject magnetic fields generated by a TLP pulse into a circuit and runs scans in both horizontal and vertical orientations to find fields generated by the resulting current.

Professor Daryl Beetner advises students who develop software models of circuit behavior.

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Other equipment includes a mechanical arm that can hold an ESD gun and move it to a device under test. Students use the arm because they can program it to achieve repeatable distances from the device. Students often use it to test handheld devices such as cellphones and MP3 players.

Obtaining equipment

The lab also includes one semianechoic chamber, one shielded room, several network analyzers and spectrum analyzers, a direct-contact probe station for working with very fine-pitch components, and some specialized equipment assembled in the lab that measures ESD and near-field radiated emissions.

The laboratory has equipment for making swept-frequency measurements of two-port parameters, impedance and materials characterization, radiated emissions, and ESD. These facilities cover the range of 100 Hz to 20 GHz. A four-port network analyzer and test set also lets students and faculty make balanced differential S-parameter measurements. Time-domain measurement equipment includes high-speed digital oscilloscopes for measuring signals with subnanosecond rise times and for time-domain reflectometry characterization of signal paths.

Over the years, test-equipment manufacturers and EMC Consortium members have come through with donations and substantial discounts to equip the lab. For example, ETS-Lindgren donated a shielded room, and Advanced Micro Devices donated an ETS-Lindgren semianechoic chamber. Each chamber is large enough to permit a 1-m distance between the EUT and a transmitting or receiving antenna. "We don't use the chambers to make compliance measurements," said Van Doren. "We use them to make baseline measurements, then make comparisons after design changes to verify their effectiveness."

Both chambers had to be disassembled at the donor facilities and reassembled in Rolla. Research technician Kenny Allison noted that "disassembling a chamber is more difficult than assembling one." The semianechoic chamber, which had ferrite tiles glued onto its walls, wasn't built to be moved, so Allison had to cut through the tiles to reach the joints be-

tween the walls, then reinstall the tiles during reconstruction.

Professor James Drewniak, who has been a self-proclaimed "loud voice" for the lab, has taken on the role of fundraising and equipment acquisitions. He came to the University of Missouri–Rolla in 1991. Drewniak, along with Van Doren and Todd Hubing (now at Clemson University), was looking for a niche because "everyone was doing computational magnetics and we needed to do something else."

To get the lab equipped, Drewniak approached several companies. Bill Curran at Lindgren (now ETS-Lindgren) donated a shielded room worth $30,000. Mike Hart of EMCO (also now ETS-Lindgren) donated $20,000 worth of antennas. Tektronix sold oscilloscopes, spectrum analyzers, and time-domain reflectometers to the lab at cost. Hewlett-Packard and later Agilent Technologies have also provided oscilloscopes, signal sources, and network analyzers at cost. "The EMC community has been very good to us," said Drewniak with a smile.

Van Doren added "We can always use a few more 1-GHz oscilloscopes. They're fast enough for measuring noise in power supplies and for many other student projects. A lot of equipment has 20-MHz clocks, and we can use 1-GHz oscilloscopes to measure clock harmonics."

Besides bringing in funds, Drewniak brings in students from all over the world. "Missouri S&T students come to the lab when they hear about us as undergraduates. Each year, we put out a call for student projects."

Students from China learn about the EMC program through professors at their undergraduate universities. "We have colleagues at several universities in China who send us students," said Drewniak. Numerous other students come from India and Europe. The ability to work with commercial companies in the Center for Electromagnetic Compatibility is another reason that students travel to Rolla to study. Those company members often hire the lab's students after graduation.

The students usually take classes in the morning, then work in the lab during afternoons and evenings. Drewniak noted that much of the lab's funding is used to pay for student stipends and tuition.

Programs such as the one at Missouri S&T produce engineers who will solve EMC problems in ICs, boards, and systems. Those problems will only get more difficult to solve as clock speeds increase and circuits shrink. Missouri S&T EMC lab graduates will solve many of those problems, which will result in safer and more reliable electronic products. T&MW

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3. IEEE International Symposium on Electromagnetic Compatibility. www.emc2010.org.

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POWER *to the* OPENS

As circuit-board complexity increases, identifying structural defects such as opens and shorts represents a significant manufacturing challenge.

BY ANTHONY J. SUTO, TERADYNE

Ever-higher bus speeds and logic densities on today's PCBs (printed-circuit boards) enormously complicate the board-test task. In particular, identifying structural defects such as opens and shorts represents a significant challenge. Today's boards are more likely to contain opens and shorts than did their predecessors, and high node counts make finding these defects considerably more difficult.

In recent years, many companies have turned to a capacitance test as a way to find opens on digital devices during in-circuit test. The technique involves placing a sensor plate on top of the device package to form a capacitor of 10 to 100 fF between it and the board node in contact with the bed of nails (**Figure 1**). (See "How capacitance test works," p. 35.) Unfortunately, the evolution of some board technologies has reduced the usefulness of the conventional capacitance technique. Maintaining bed-of-nails access has become increasingly difficult for designs that include ball-grid arrays, flip chips, and other high-density devices that defy conventional probing. Even when access is theoretically possible, the force required to make sufficient contact to test numerous pins in a small area can exert stresses on the board that can cause damage to the solder joints or to the board itself.

Improving bed-of-nails access to the nodes on the boards has generally involved adding test pads as contact targets, but such test pads occupy precious board real estate. In addition, signal speeds are constantly rising, and adding a test pad to a particular length of signal etch increases trace capacitance, creating a nonuniform impedance for the overall signal path. Such variations along the transmission line can cause reflections and other signal degradation when the board is running in high-speed mission mode.

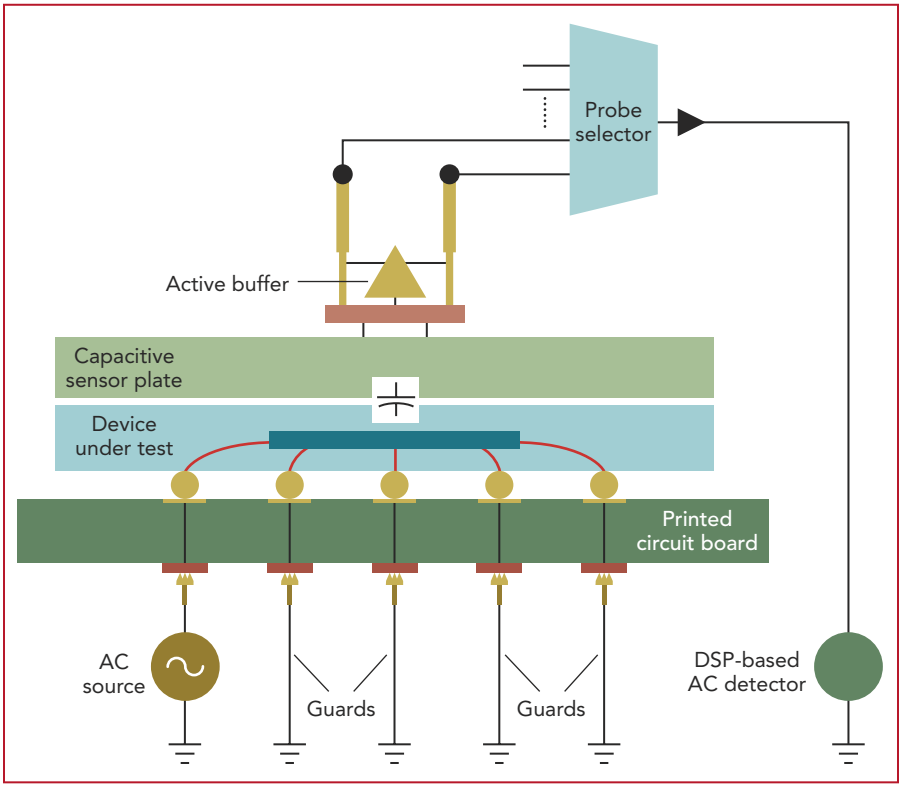

FIGURE 1. A traditional open-pin detection technique employs a capacitive sense plate.

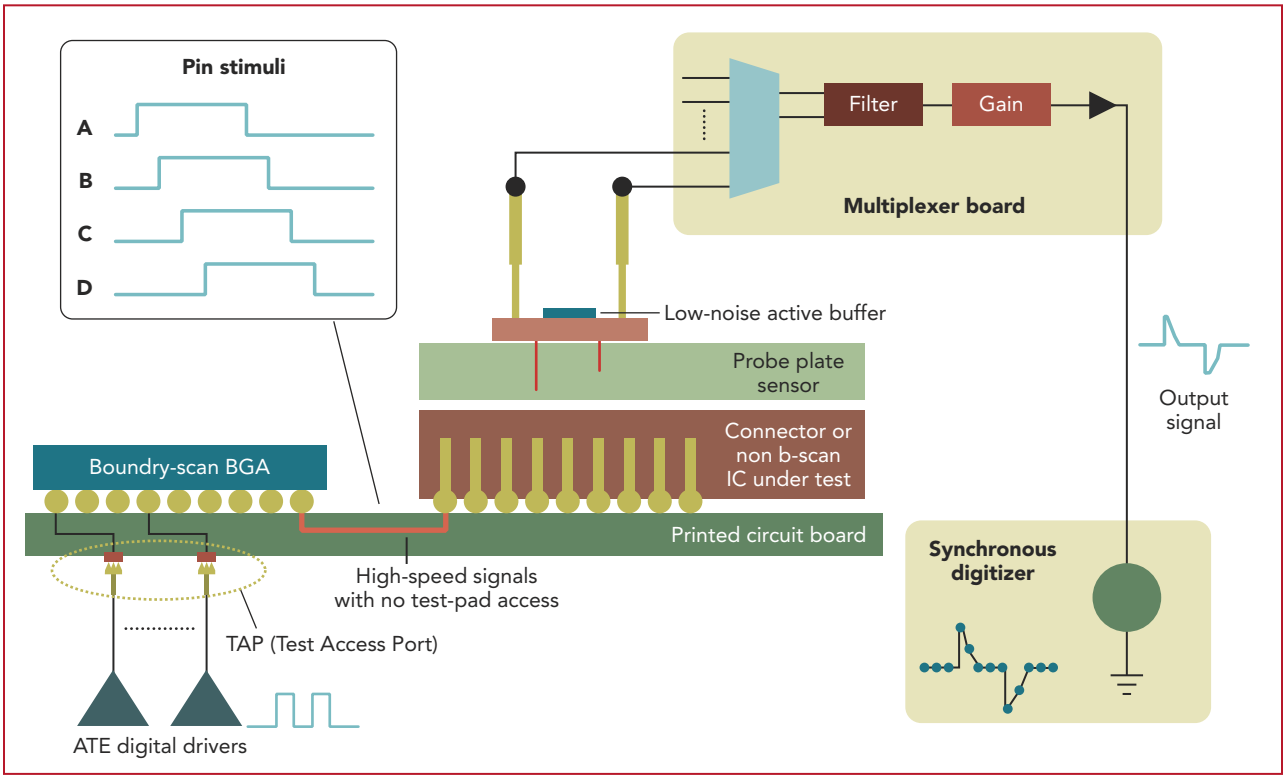

FIGURE 2. The open-pin detection scheme depicted here employs boundary scan as the stimulus source.

Taking advantage of boundary scan

You can improve upon the capacitance-based test by supplementing it with boundary-scan (IEEE 1149) techniques. Many complex devices contain boundary-scan circuitry, allowing access to their I/O structures through a four- or five-pin TAP (Test Access Port). If all devices on a board contain boundary-scan circuitry, the interconnections can be verified using boundary-scan test methods alone. Of course, not all devices offer such a luxury, and the ones that do are often connected to unpopulated connectors or empty sockets during in-circuit test.

Although the boundary-scan circuitry can provide a stimulus signal or measure a response, passive devices cannot interact with the boundary-scan tests designed to locate process defects. A custom test device plugged into the socket or connector could channel the output signal to the tester, but employing such a device proves impractical in high-volume manufacturing. It would increase test time, and the test devices themselves would wear out and have to be replaced.

A more viable option would be to place a capacitive probe in the test fixture over the target socket or connector to easily detect opens between nodes on those devices and a boundary-scan component.

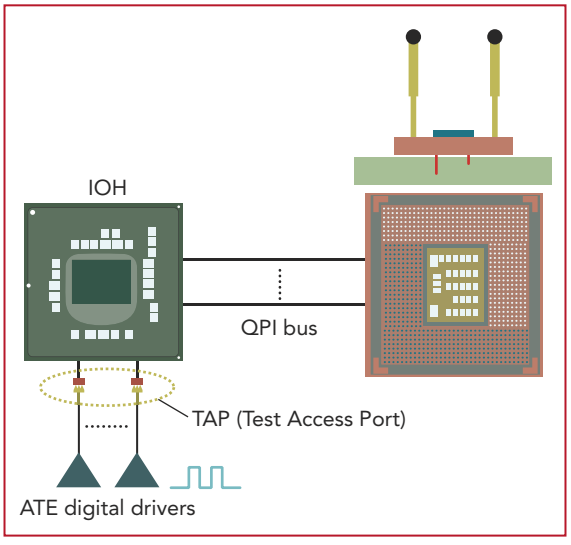

FIGURE 3. In this test example incorporating an LGA 1366 socket and an IOH chip, a TAP connects to ATE digital driver resources that generate boundary-scan commands and stimulus vectors.

The fact that the probe sits on top of the connector or socket rather than being inserted directly eliminates probe or socket wear out. This approach, which I call a "powered-capacitive test," combines the access advantages of boundary scan with traditional capacitive opens detection.

The high-level block diagram in **Figure 2** illustrates a test setup for implementing the combined approach. A tester's digital drivers connect to the TAP of a boundary-scan device, providing input signals to the boundary-scan chain that get clocked out of each of the output pins. The output stimulus consists of a single pulse per target-device pin (one rising edge and one falling edge). Whenever possible, all other DUT (device under test) pins are held at a logic-high or a logic-low to isolate the capacitive sensor plate from any other onboard activity.

The signal from the sensor plate is processed through a local low-noise transimpedance amplifier and continuous-time analog filters; it is then digitized, digitally filtered, and finally analyzed. As in

a traditional capacitance-based test, comparing the measured signal against thresholds measured on a known-good equivalent identifies any open pins.

Changing domains

To stimulate the board under test, the tester could apply a repetitive signal, such as a square wave, or a single event signal, such as a pulse. Analysis of the output signal could occur in either the time domain or the frequency domain. The powered-capacitive test method applies a nonrepetitive pulse and analyzes it in the time domain, because this combination provides significant benefits over the alternatives during production testing.

Most opens-detection techniques use a frequency-domain approach, applying a sine wave with a frequency that falls into a narrow range—typically 8 to 10 kHz—before taking a measurement. Lower frequencies reduce the capacitive reactance between the probe plate and the component under test, reducing fault coverage. Frequencies higher than 10 kHz can cause coupling between the board and the measurement plate, so a board can pass despite an open pin. This narrow stimulus-frequency range complicates the task of sending stimuli through a boundary-scan chain, because the output square-wave frequency is roughly equal to:

$$f_{TOGGLE} = \frac{TCK}{2 \cdot (\#scan\_cells)}$$

where:

- f_{TOGGLE} is the IC pin toggle frequency in hertz,
- TCK is the boundary-scan clock frequency in hertz, and
- #scan_cells is the number of boundary-scan cells in the chain.

The effects of fixture wiring in an in-circuit-tester generally limit the frequency of the boundary-scan clock to 2 MHz or less. With more than 125 cells in the scan path, generating the required 8- to 10-kHz signal becomes difficult. Most devices contain boundary-scan testability structures that can include hundreds of scan cells. Therefore, shifting signals through several such devices can easily require propagation through thousands of cells, further dividing down the toggle frequency.

Even putting all other ICs in a scan path into a bypass mode may not alleviate the frequency problem, because it would not reduce the number of scan cells below the number inside the DUT itself. Although higher tester frequencies are achievable, the necessary specialized fixture hardware would increase fixture costs.

Single-event edge-recognition techniques in the time domain overcome these limitations. A test that uses these techniques does not require a specific test frequency and, therefore, is not restricted by TCK clock frequency. The test simply generates the equivalent of a single pulse with two edges that can be placed anywhere in the vector stream, eliminating frequency-domain scan-cell-length restrictions.

In addition, the time-domain approach works well with all devices that conform to the IEEE 1149.1 and 1149.6 standards, and it does not require boundary-scan devices to support custom commands or fixtures to support additional electronics. Finally, a single pulse offers a throughput

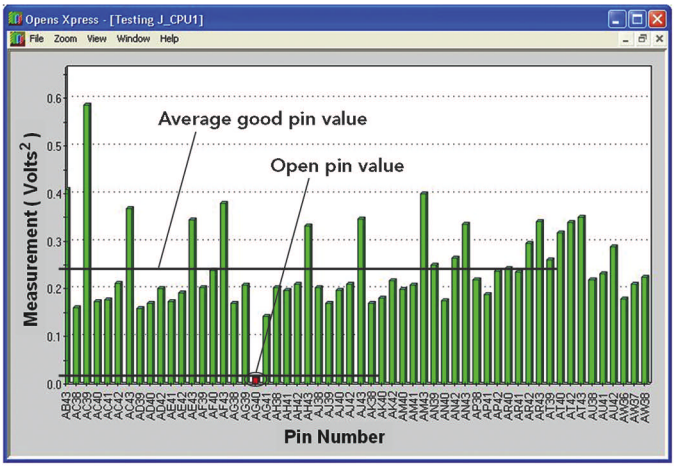

FIGURE 4. These typical test results illustrate the startling difference between a connected pin measurement and an open pin measurement.

How capacitance test works

A common diagnostic technique for finding opens on digital devices during in-circuit test involves the use of a bed-of-nails tester and a capacitance test. By placing a sensor plate on top of a device package, the tester forms a 10–100-fF capacitor between the device and the board node in contact with the bed of nails. In this technique, a low-amplitude AC stimulus applied to a board node that should be connected to a pin on the device under test propagates into the device and to the plate. A local active probe just above the plate then amplifies this signal and modulates it onto the two wires connecting the probe to the instrumentation via a multiplexer board.

The multiplexer board selects which probe to energize and translates the current signal on the two lines to a voltage equivalent. A continuous-time analog filter removes noise components from the voltage signal. Another function block amplifies it.

Applying a DFT (discrete Fourier transform) to the result removes additional noise components and produces a frequency-domain signal whose amplitude corresponds directly to the capacitance of the circuit path. Measuring that capacitance on known-good boards establishes a baseline for the subsequent production test.

An open on the board acts like an additional capacitor in series with the first. The device leadframe and sensor plate form one capacitor; the pad and trace on the circuit board form the other. The air gap caused by the open serves as the dielectric, producing about 25 fF of capacitance. The equivalent capacitance of the open circuit will be much lower than if the pin were properly connected, unambiguously identifying the defect. The same approach can be used to find opens on unpopulated sockets and connectors as well.—*Anthony J. Suto*

advantage over a repetitive test signal. Throughput typically improves by 50% to 400%, depending upon the number of scan cells in the chain and the number of cells that are actually being tested.

Unfortunately, the time-domain technique has some drawbacks. A repetitive signal such as a square wave of known frequency in the presence of noise can easily be averaged over time to reduce the unwanted noise components. Using a DFT (discrete Fourier transform) to measure a single tone, the equivalent noise bandwidth is proportional to the digitizer's sampling rate (Fs) divided by the number of samples (N). Because dimensionally this quantity is reciprocal time, measuring the signal over a longer time produces a narrower DFT bandpass filter with less noise in the measurement. The only downside is the added test time required to integrate stochastic noise to a lower value.

In contrast to a square wave, a single pulse consists of a positive step followed by a negative step that can be spliced together later. Measuring the rich harmonic content in this single pulse requires significantly more bandwidth than is required for measuring the fundamental frequency of a square wave. This additional bandwidth admits additional noise to the system, increasing the measurement's standard deviation, requiring a technique for removing the noise from the signal to make the measurements more repeatable.

Such a technique can be found in the world of radar systems. The method, called "matched filtering" or "optimal filtering," correlates a known signal or template with the measured signal in the presence of environmental noise, as defined by this equation:

$$R(d) = \sum_{i=0}^{K} [(X(i) - Mx) \cdot (Y(i) - My)]$$

where:

- X(i) and Y(i) are the data vectors,
- Mx and My represent the mean values of those vectors, and
- R(d), which is the cross-correlation coefficient, denotes the likelihood that the measured signal matches the reference signal both in temporal response and in magnitude.

Knowing the shape and amplitude of the signal you are trying to detect ahead of time, you can apply a matched filter to significantly reduce the noise components largely attributed to the increased signal-path bandwidth.

Determining whether a node is open requires first performing a de-normalized autocorrelation through the learn process on known-good boards. One way to do this is to calculate a mean and standard deviation from several autocorrelation values and determine whether there is any undesirable variation caused by surrounding noise and whether the magnitude is too small. You should average the learned vectors to create a final autocorrelation coefficient and a refer-

ence vector. When the autocorrelation value is compared with the results from the cross correlation during production test, any deviation greater than a maximum percentage or less than a minimum percentage will indicate a defective pin.

In addition, because the board is powered during the test, noise coming from locations on the board away from the node under test can reduce the measurement's signal-to-noise ratio. This phenomenon is common to both the time-domain and the frequency-domain techniques, so you must carefully manage it regardless of which approach you select.

An example

Consider the test setup for the Intel LGA 1366 server-board processor socket shown in **Figure 3**. The left side of the figure shows an I/O controller hub IC (IOH) with boundary-scan capability.

The TAP is connected to the ATE (automated test equipment) digital driver resources, which will generate the required boundary-scan commands as well as the stimulus vectors. A QPI (quick-path-interconnect) bus operating at 6.4 Gbps connects the IOH chip to the processor socket. Without node-pad access, testing this configuration requires the powered-capacitive technique.

The capacitive sensor plate above the LGA 1366 pin field detects the output signals and, in combination with the boundary-scan device, can identify open connections. **Figure 4** shows some typical results; note the significant difference between a connected pin measurement and an open pin measurement. The average of the pin measurements is a little less than 250 mV^2, as shown by the upper horizontal line in the figure. Faulty pin AG40 shows up in this graph as a small red bar. The average connected pin values differ from the open pin value by a ratio of about 10:1. (The data in the graph represent the output value for each pin after processing the raw temporal data through the time-domain algorithms, rather than an amplitude reading that would come from a conventional analog opens measurement.)

The combined key attributes of boundary-scan and capacitive-based opens techniques extends in-circuit test coverage in the presence of limited access to test pads and on densely populated boards that cannot afford test-pad real-estate. Using a single event pulse as a stimulus and analyzing the test results in the time domain eliminates the major drawback of an upper boundary-scan cell limit when testing complex PCB assemblies. Boundary scan and capacitive opens have quietly co-existed for nearly two decades. By giving "power to the opens test," a unique technology marriage will facilitate testing complex boards for years to come. T&MW

Anthony J. Suto *is Teradyne's chief scientist responsible for the Assembly Test Division's ICT and AXI technologies in North Reading, MA.*

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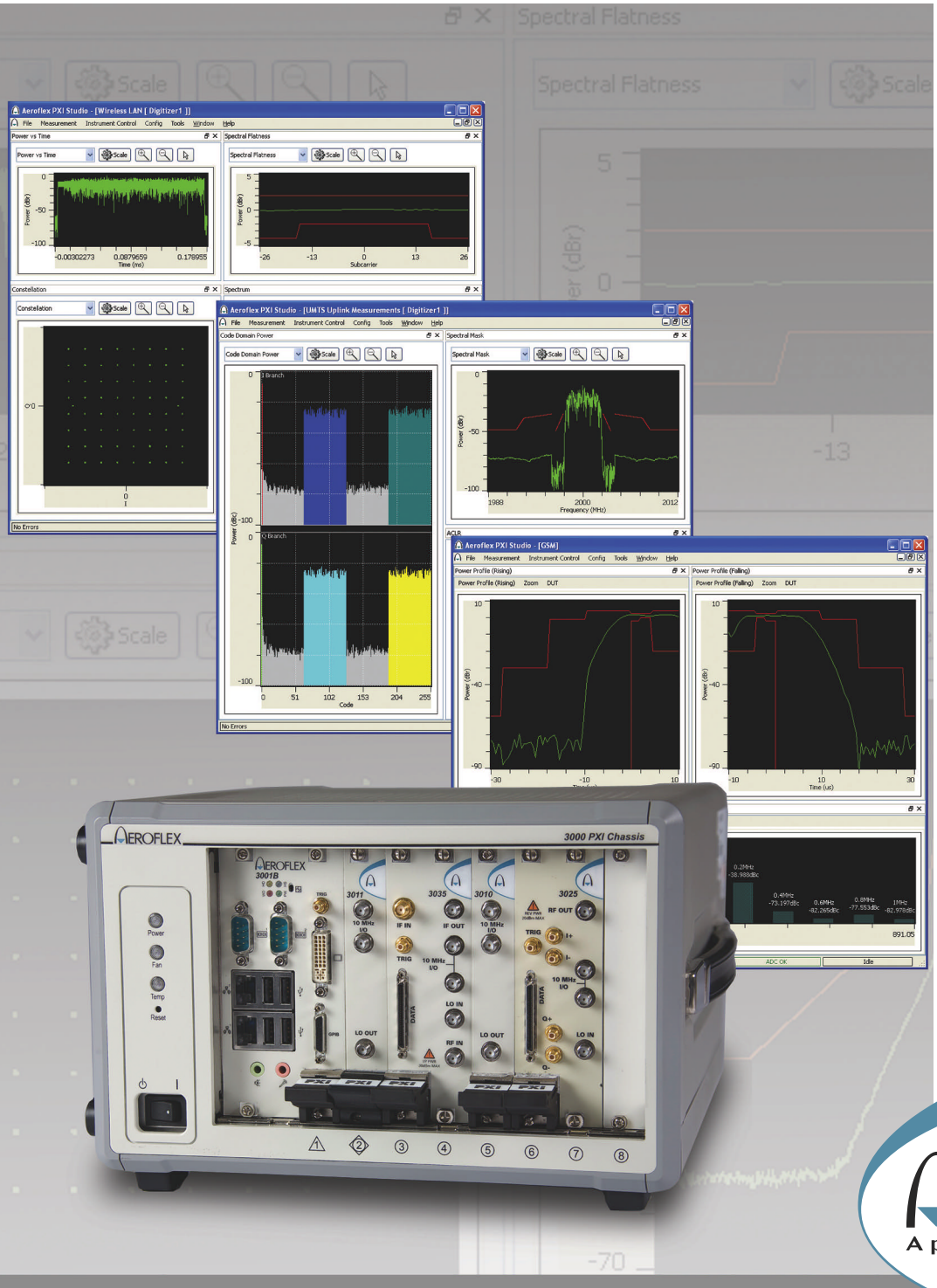

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PXI expands processing potential

By Richard A. Quinnell, Contributing Editor

With last November's release of the PXI-7 (hardware) and PXI-8 (software) specifications—collectively called PXImc (PXI Multi-Computing)—the PXISA (PXI Systems Alliance) standardized the implementation of multiprocessing in PXI systems. For PXImc, modules connect to the PXI host system through a nontransparent bridge. The goal was to provide a high-bandwidth, low-latency interconnect between computing devices in either a modular or standalone system configuration. I spoke with Mark Wetzel of National Instruments, who is chairman of the PXISA technical committee that developed the standards, to find out what test engineers should know about PXImc.

Q: What prompted development of the PXImc specifications?

A: The introduction of PXI Express triggered a growing need for increased processing power in PXI systems. There were also needs for multiprocessing coming out of the synthetic instruments group. So, about two years ago, the technical committee began looking at ways to add multiple CPUs for data processing to a PXI platform.

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Q: What issues needed addressing?

A: On the hardware side, we wanted to ensure that existing PXI Express hardware would work in a PXImc configuration without needing modification. That drove decisions about where the bridge chips are located, how clocking is handled, and how to set up cabling for connection to external devices. On the software side, the key considerations were to ensure that multivendor hardware configurations and hardware substitutions would work without problems and to ensure that the software had minimal overhead so it wouldn't compromise the bandwidth and low latency of the PXI Express links.

Q: How do the specifications ensure this kind of interoperability?

A: There are two pieces that ensure interoperability. One provides a shared software component for PXImc devices that developers get from the PXISA, which gives users an API [application programming interface] that will work with all vendors' implementations. The user interacts only with the shared component, even though there may be vendor-specific software below it. The second piece ensures that the software masks any differences in nontransparent bridge hardware implementations.

Q: Any unusual challenges arise in creating the specifications?

A: One thing we did that was unusual for the PXISA is that we wanted to go beyond the PXI chassis to connect to things like external PCs and other box instruments. The nontransparent bridges used to connect to PXImc systems`are not used just in PXI; they appear in other platforms as well. We wanted users to be able to connect these other platforms to PXI just as easily as PXImc. This gives engineers the best of both worlds: the ability to integrate a system into a single chassis or use external system components for highest performance.

Mark Wetzel
Chairman
PXISA Technical Committee

Q: Any advice for test engineers considering PXImc?

A: There is information in the specifications on where logos and markings are to be placed that is important to follow. The PXImc cables do not guide connections the way USB cables do, so users need to know where the bridges are located and in which direction signals are flowing in order to configure their systems properly. That's what the labeling provides. It's also good to understand that PXImc is an enhancement to PXI. There are plenty of applications that will not need it. Instrument suppliers will be able to give users good guidance on where PXImc will be most valuable. □

GUEST COMMENTARY

PXI and electric transportation

By Bob Stasonis, Pickering Interfaces

With our depleting petroleum stocks, it is clear that the transportation scene for most people in the world is changing. The next big "thing" in transportation will likely be electric vehicles, be they resort shuttle carts, warehouse forklifts, hybrid vehicle systems, or full electric vehicles—even subway trains are electric. J.D. Power predicts that hybrid vehicle production for the US market will exceed 1.4 million vehicles by 2015. Add to that the electric vehicles at resorts, in distribution centers, and under the city, as well as devices like the Segway, and you're talking about a lot of batteries to charge.

This paradigm shift in transportation technology calls for advances in power systems and in the ATE (automated test equipment) systems that make sure a vehicle works before you step on the accelerator. Fortunately for the test engineering community, PXI is up to the task.

For example, several PXISA (PXI Systems Alliance) members offer switch modules that have the performance needed for the high voltages—greater than 300 V—in the battery stacks. There are also sensor-emulation PXI modules that can help test a vehicle's BMS (battery-management system)—the complex circuit that addresses the charging and monitoring of the many battery cells that make up a stack. The sensor-emulation modules simulate temperature monitors in the stack, and high-density switch matrices are used to inject signals and faults and monitor the response of the UUT (unit under test). Add battery simulators, CAN communication modules for querying the BMS and running diagnostics, and digital multimeters for performing voltage checks, and you have a complete test system in PXI.

In addition, the small size of PXI test systems makes it more convenient to use them in areas such as environmental chambers, allowing the systems to be as close as possible to the UUT during product development and also during HALT (highly accelerated life testing) and HASS (highly accelerated stress screening) applications.

As emerging technologies call for new test techniques, the PXISA community will clearly be ready with solutions. Just as PXI has been used for applications in the internal combustion engine arena for over 10 years, PXI will be addressing the testing needs of the electric transportation industry for years to come. □

Bob Stasonis *is the sales and marketing manager for Pickering Interfaces.*
bob.stasonis@pickeringtest.com

HIGHLIGHTS

Suite tests TD-SCDMA handsets

The PXI 3030 TD-SCDMA Measurement Suite from Aeroflex is designed for the testing of mobile handsets and RFICs based on ETSI 3GPP TS 34-122. The suite works with the company's PXI 3000 series instruments, which currently support 3GPP LTE, CDMA2000, 1xEVDO, GSM, W-CDMA, and mobile WiMAX, as well as WLAN and Bluetooth; Aeroflex says that customers can use software upgrades to add the TD-SCDMA standard to their PXI 3000 test systems.

"Aeroflex is targeting the rapid growth in demand for TD-SCDMA cellphones with our new test suite," said Tim Carey, product manager, PXI 3000 Series, in a prepared statement. "With the total number of Chinese cellphones exceeding 300 million units, the need for high-throughput test systems is vital to manufacturers who need to keep up with the growth in China."

The PXI Measurement Suite makes parametric measurements of TD-SCDMA transmitters and supports high-speed alignment and performance verification of devices operated in a nonsignalling mode. The suite can be used in testing of high-speed and high-throughput mobile handsets as well as in RFIC characterization. The TD-SCDMA Measurement Suite is compatible with any Aeroflex 3030 Series RF digitizer. www.aeroflex.com.

Pickering expands PXI offerings

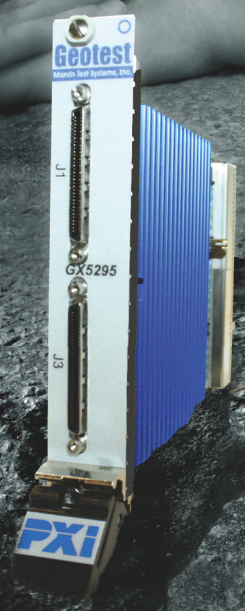
The new 41-924-001 interface kit from Pickering Interfaces provides a seamless connection between a PC's PCIe (PCI Express) bus and a PXI chassis backplane. The kit contains a single-lane PCIe card, a connecting lead, and a PXI module for insertion into Slot 1 of any PXI chassis; it is an alternative to the company's 41-921-001-KIT, which uses a PCI slot rather than a PCIe slot in the PC.

The company has also announced the 40-873 (50-Ω) and 40-833 (75-Ω) multiplexer modules that feature one or two 4:1 multiplexers with terminated inputs in a single PXI slot. The modules are designed for switching applications up to 3 GHz.

Pickering's new 40-555 solid-state 8x2 switch matrix is a two-slot PXI module that features a 30-A current rating and high inrush current tolerance. In addition, the company has added the 40-160-003 to its 40-160 switch matrix line. The single-slot PXI module supports 20 SPST 10-A relays and is suited for switching DC signals up to 30 V and AC voltages to 250 V. www.pickeringtest.com.

Something New Emerges in PXI

Geotest
Marvin Test Systems, Inc.
www.geotestinc.com



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Battery Management Systems Testing?

Pickering Interfaces has all the hardware you need

As more and more hybrids/plug-in hybrid vehicles are introduced, the testing of the Battery Management System, or BMS, is becoming an important part of an automobile's manufacturing process. The ability to simulate problems such as overcharged, shorted, or failing cells while testing the entire system response is crucial to validating a safe BMS. That is why Pickering has introduced the 41-752, the only multi-channel battery simulator in PXI. In addition, Pickering has 1 kV switching, Sensor Emulation using our precision resistor family, DMMs, and CAN Interfaces - everything you need to create the perfect BMS Test System. Contact your local Pickering sales representative or go to pickeringtest.com and see why Pickering Interfaces should be an integral part of your BMS test strategy.

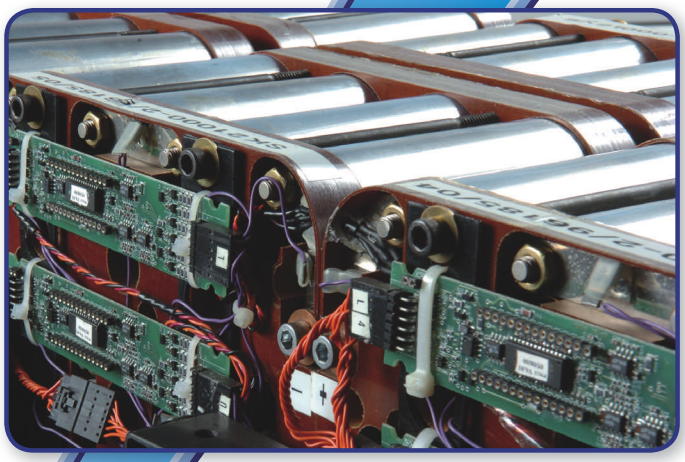

*Photo courtesy of Argonne National Laboratory

41-752
6 Channel Battery Simulator Module

PXI

PXI Chassis with sixteen 41-752s, simulating 96 cells of a Lithium Ion battery stack.

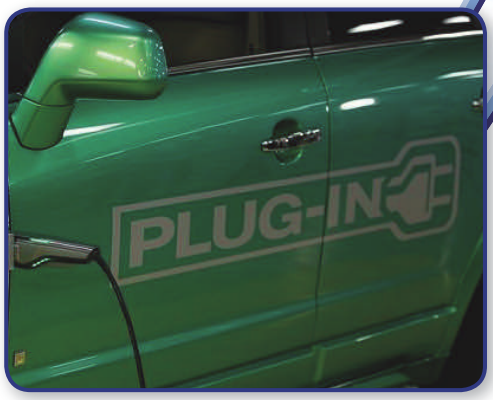

*Photo courtesy of www.electriclithiumbattery.com

41-500
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24 x SPST High Voltage Power Relay Module

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41-210
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User-configurable FPGA modules boost PXI system versatility

By Richard A. Quinnell, Contributing Technical Editor

The advent of PXI Express created new opportunities for PXI systems to handle more data faster. Module developers turned to the FPGA (field-programmable gate array) as a hardware-configurable alternative to high-speed or multicore CPUs for handling this data. Now, such FPGA performance and configurability is becoming available to system developers and end users, adding a new range of design possibilities for PXI systems.

PXI module developers began using FPGAs in their high-performance designs nearly a decade ago to handle ever-increasing data rates and to reduce latency. The configurable hardware offered significant performance advantages over software-based designs. Sebastien Maury, Sundance Multiprocessor Technology's regional director for the Americas, estimated that an FPGA can provide 20X to 30X more digital processing performance than a PXI host controller.

Ryan Verret, FPGA-for-Test product manager at National Instruments, said the performance boost can be even greater, up to several orders of magnitude. "It's really staggering what computation you can do on an FPGA," he said. "Some devices have more than 500 DSP blocks on them, allowing you to do lots of FFTs [fast Fourier transforms] in real time."

Flexibility has been another reason for incorporating FPGAs into module designs. David Manor, VP of hardware engineering at Geotest—Marvin Test Systems, pointed out several advantages that stem from field configurability: "Using FPGAs allows us to get products that relate to new standards out early, even before the standards are fully defined. We have to make some assumptions, so we may not get everything exactly right at first, but [we] can release updates and bug fixes for users to download without the need to return their boards to us."

The use of FPGAs also simplifies the creation of unique functionality for customers. "The customer simply installs new firmware to gain new features," Manor said. He pointed out that the ability to upgrade and modify module functionality in the field helps keep Geotest's products viable longer in a given application. "This extension of a module's useful life is really good for mil/aero applications, which need a design lifetime of at least 10 years."

User-configurable FPGA modules arise

Until recently, however, the FPGAs in PXI modules have been nearly inaccessible to the end user. Upgrades and enhancements came from the module vendor, and users could not readily implement their own design ideas. That changed in the last year with the introduction of user-configurable FPGA modules for PXI from at least four manufacturers: Geotest, NI, OpenATE, and Sundance.

The Geotest GX3500 PXI module connects 160 digital I/O channels to an Altera Cyclone III FPGA having 55,000 logic elements, four PLLs, and 2.34 Mbits of memory. The FPGA has access to all PXI bus resources, including clocks and triggering. The module also supports an internal expansion card assembly that customers can use to customize the front-panel I/O connections (**Fig. 1**).

NI offers a family of FPGA modules called the FlexRIO series that use Xilinx Virtex-5 FPGAs of varying capacities. The NI PXI-795x series consists of conventional PXI modules, while the PXIe-796x series instruments are PXI Express modules. FlexRIO modules offer 132 I/O lines and accept front-panel-mounted adapters that customize the I/O interface for connection to analog, Ethernet, IEEE 1394 (FireWire), Camera Link, and other specialized interfaces (**Fig. 2**). Adapter modules are available from NI as well as from third-party partners such as Adsys Controls, Averna, NexFrontier Solutions, and Prevas.

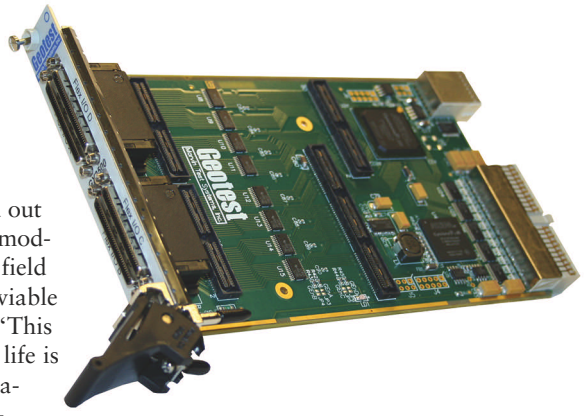

Fig. 1 The GX3500 FPGA module provides space for an internal daughter card to customize I/O signals without exceeding the envelope of a standard 3U module.
Courtesy of Geotest—Marvin Test Systems.

OpenATE also uses a Xilinx Virtex-5 FPGA on its FPGA carrier card. The OpenATE card offers a more basic design than those from Geotest and NI, however, with the FPGA handling the PXI bus interface instead of requiring a separate interface device. The company does provide PXI interface IP, however, as well as IP for a DIMM interface. The FPGA carrier supports a user-defined daughter card that handles 156 I/O lines but provides no built-in front-panel connections. Users must customize the front panel along with the daughter card.

The Sundance SMT-700 FPGA card offers a PXI Express interface, a variety of front-panel serial interfaces, and internal digital I/O headers along with a choice of several different Xilinx Virtex-5 devices. Front-panel serial interfaces include 10/100/1000

Ethernet, fiber optic, and USB. Dual internal mezzanine connections allow developers to attach Sundance analog modules or additional digital I/O to the FPGA card. The connections are located on both sides of the board, causing the FPGA card to occupy two PXI slots when populated.

Daughter cards customize I/O

While these FPGA modules have significant differences, they do share some attributes. For example, each of them can be converted from a simple data-processing card into a fully defined instrument with the addition of customization circuitry, through either a mezzanine card or an extension card. The FPGA module vendors offer both predefined cards and open specifications from which users can develop their own cards. This ability to define the module's I/O signal conditioning and formatting combines with the FPGA's configurability to give users an unprecedented opportunity for creating innovative PXI module functions from off-the-shelf building blocks.

Fig. 2 The FlexRIO series FPGA modules use external adapter modules for I/O customization and are available in both PXI and PXI Express versions.

Courtesy of National Instruments.

An FPGA module with high-speed ADCs on the customization card, for instance, has all the hardware needed to serve as a digital spectrum analyzer. Because of the tremendous parallelism available in the FPGA, that analyzer can provide continuous monitoring across a wide frequency band in place of the usual swept-spectrum analysis. As NI's Verret pointed out, this allows the FPGA-based instrument to analyze time-multiplexed communications protocols such as RFID that use short energy bursts. Swept-spectrum instruments can easily miss these bursts.

Verret also noted that the continuous monitoring allows an FPGA-based instrument to generate triggering signals based on complex power-frequency spectrum masks. This can be helpful in reducing the capture-depth requirements of downstream data-acquisition systems.

Developers can also configure an FPGA module to generate test signals dynamically, reducing the number of test vectors needed in an ATE (automated test equipment) system. For example, when a conventional ATE system needs to send data to a communications port on an IC under test, the system must use a long series of test vectors to drive arbitrary waveform generators that produce the signals driving the port. These vectors must describe the signal values at every time step throughout the duration of the data transfer and can be quite long. By using an FPGA, developers can create a state machine that will control the signal timing so that the test vectors only describe data values to be transferred and not the signal's entire time history.

Dynamic signal generation also allows an FPGA-based instrument to handle situations that are difficult or impossible to handle with static vectors. Testing of RFID devices, for instance, is difficult with static vectors because the multiple stimulus-response interactions involved may have variable timing. Similarly, the testing of an engine-control module requires that the tester emulate how the engine and drive shaft will behave in response to the control signals. Such responses are virtually impossible to emulate with vectors, and host-controller-based emulation is often too slow or has too much latency. An FPGA-based emulator can resolve all these issues.

FPGA modules can even adapt their functionality on the fly. According to Sundance's Maury, systems can partially reconfigure an FPGA while the module is running to change its behavior in response to incoming signals. Such dynamic changes might include altering test vectors to more extensively test functions that appear marginal, or automatically revising signal-processing algorithm parameters to tune them for the current test conditions.

Vendors provide development support

The extreme flexibility that user-configurable FPGA modules provide PXI developers does come at a price. NI's Verret, for instance, pointed out that designing the logic of an FPGA may not be within the skill set of many test engineers because of the need to work with an HDL (hardware description language) to define their designs. "Even if they have the skills," said Verret, "it [configuring an FPGA] is harder to do than writing processor code." To minimize the FPGA configuration effort, most module vendors offer development support.

NI, for instance, has created an FPGA Module extension for its LabView development tool. This extension allows developers to describe their entire test-system design and data-processing algorithms in LabView and have the tool automatically prepare the FPGA programming code. The company is also providing a library of IP for more complex, application-specific functions. NI's third-party partners offer additional IP as well as full turnkey solutions.

Geotest has made its FPGA module fully compatible with standard Altera object files. This means developers can use the free Quartus II Web Edition development tools that Altera provides in support of its FPGAs

rather than needing proprietary toolsets. Geotest also provides drivers and a virtual panel for interactive design, debug, and deployment of the FPGA configuration. Interface files for this tool support programming tools and languages such as ATEasy, C/C++, Visual Basic, and LabView. The company offers an online tutorial to help developers get started.

Sundance, which caters to more experienced hardware design customers, provides only some basic software to developers. For full development support, the company works in partnership with software company 3L. The 3L Diamond toolset allows developers to create a task-based model of the FPGA's function, and it then automates the design's compilation to FPGA programming vectors. It also supports the synchronization of multiple FPGAs for achieving extended performance through multiprocessing. Developers can also use a tool such as The Mathworks Matlab to capture their design and convert the tool's output to an HDL for compilation using Xilinx tools.

Will a user-configurable FPGA help you?

While the level of programming involved in customizing a user-configurable FPGA module for their unique application may be daunting to many PXI users, the results can be well worth the effort. The key is deciding if the effort is necessary.

NI's Verret recommended that users consider an FPGA module if they can benefit from custom triggering that will reduce the amount of data the host controller must process and when data-processing requirements demand the performance provided by an FPGA. Geotest's Manor said that the use of an FPGA card is justified when there is nothing available to support a special function that an application requires or when there is a need to change functionality on the fly, such as while running a test.

Ultimately, customer feedback will determine the long-term future of these user-configurable PXI modules. Vendors anticipate continuing to offer larger, faster FPGAs as they become available and will likely create additional daughter cards and IP based on the frequency of customer requests.

But even if the FPGA module remains only a specialty item, the future of FPGAs in stock PXI instrument modules is secure. "We couldn't be where we are today in PXI without FPGAs," said Geotest's Manor. "They have been a key component in the success of PXI as a performance platform." □

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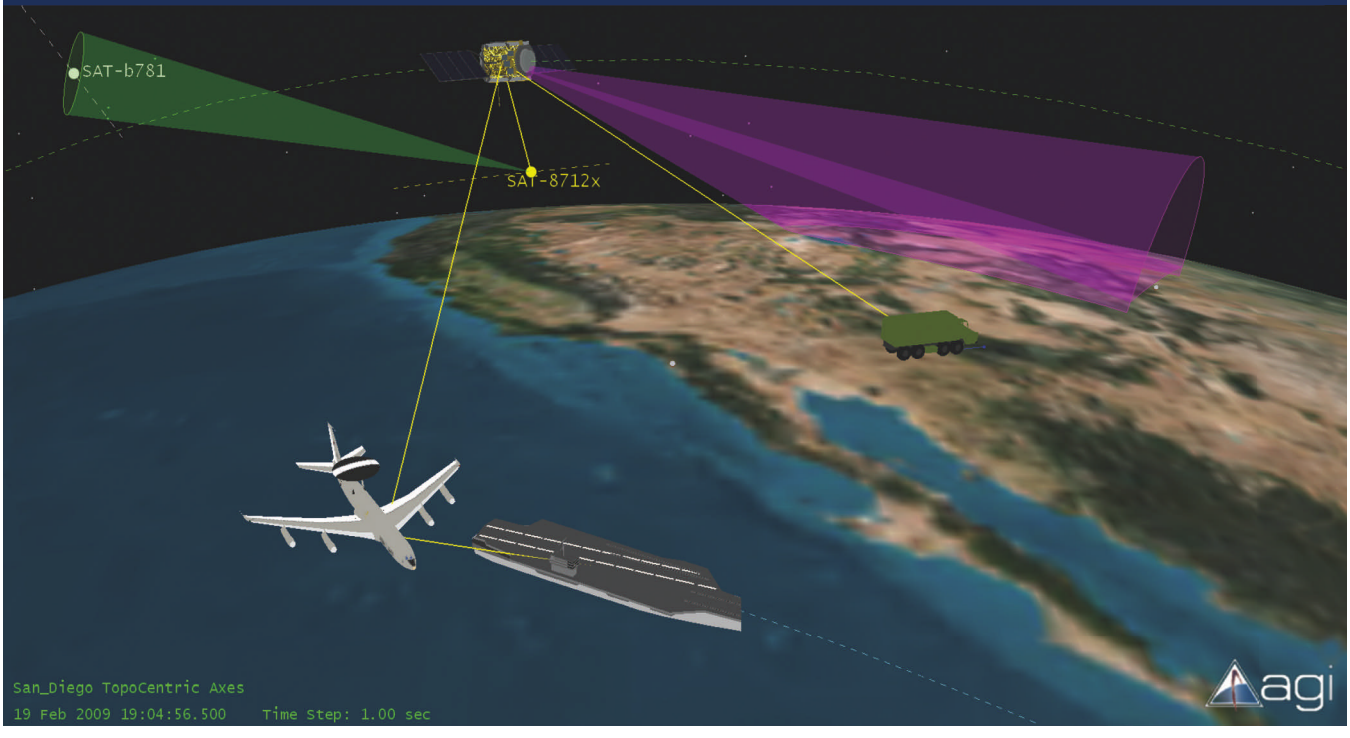

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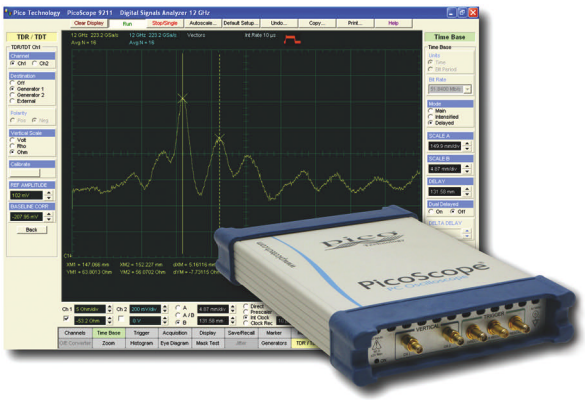


USB oscilloscope adds TDR analysis

The PicoScope 9211A USB oscilloscope includes TDR (time-domain reflectometry) and TDT (time-domain transition) analysis. With TDR/TDT analysis, you can use the 12-GHz sampling oscilloscope to characterize signal paths such as PCB traces, connectors, and cables. The instrument produces pulses with 100-ps rise times and then measures the response.

The PicoScope 9211A also performs mask-limit testing for communications standards such as SONET/SDH, Fibre Channel, Ethernet, InfiniBand, XAUI, RapidIO, PCI Express, and Serial ATA. It has three trigger inputs: a DC to 1-GHz direct trigger, a 1-GHz to 10-GHz prescaled trigger, and a 12.3-Mbps to 2.7-Gbps clock-recovery trigger. It also has a 10-Gbps pattern-sync trigger for averaging eye diagrams. The 9211A can also perform histogram analysis on waveforms to characterize jitter distribution. The 9211A comes with calibrated cables, filters, power splitters, and adapters.

Price: £7,495 (approximately $11,500). *Pico Technology, www.picotech.com.*

Instrument calibrates DC measurements

The Model 526 precision DC voltage/current source/calibrator lets you calibrate measuring devices such as ADCs and dataloggers. Its four voltage ranges (±100 mV, ±1 V, ±10 V, and ±100 V) and resolutions from 100 nV to 100 µV let you calibrate a wide range of products. The instrument can source current in a ±10-mA range and a ±100-mA range. A carry-and-borrow feature lets you change ranges without an interruption in output.

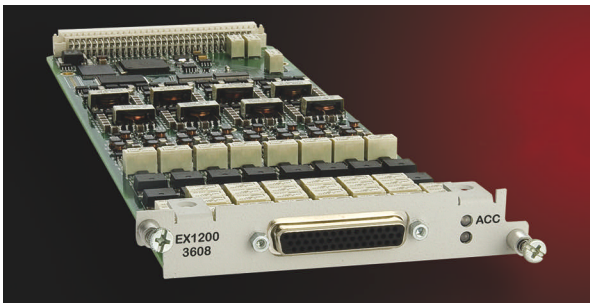
The instrument has five gold terminals on the front panel for bench testing and a six-pin Amphenol military-style connector on the rear panel for production use. The terminals provide four-wire source-and-sense connections plus ground. You can operate the Model 526 from the front panel, through stored settings, or remotely through the GPIB and Ethernet ports.

Price: $3750. *Krohn-Hite, www.krohn-hite.com.*

VTI adds analog-output modules

VTI Instruments has expanded it EX-1200 chassis and card-based instrument line with two analog-output modules: the eight-channel EX1200-3608 and the four-channel EX1200-3604. All outputs are differential with 100-V isolation, which minimizes noise caused by ground loops. You can use any channel as a static voltage output or as a 400-ksamples/s arbitrary waveform generator. Each channel includes a pair of sense lines so you can verify the output at the device under test, thus eliminating errors produced in current-carrying wires.

Each output on the EX1200-3608 and EX1200-3604 has ±20-V, ±10-V, ±1-V, and ±0.1-V output ranges. You



can connect channels in series when you need voltages above 20 V. Each channel can source up to 20 mA. You can build waveforms with the modules' 1 Msample of memory and program them with loops and branches to increase effective waveform length. The instrument cards let you store up to 4096 unique signal patterns.

Prices: EX1200-3604—$1200; EX1200-3608—$2400. *VTI Instruments, www.vtiinstruments.com.*

Kelvin test contactor is reconfigurable

Built to accommodate pad-style IC packages, the Pad ROL 200K (Kelvin) test contactors from Johnstech can be used to test high-power analog devices that require tight test guard-bands. The Kelvin-ready design allows you to configure and reconfigure the test socket for standard contacting, selective Kelvin testing, or full Kelvin testing.

(continued)

The Pad ROL 200K employs a solid-force contact and a dual-touch sense contact to guarantee a high-current, low-resistance connection, regardless of device contact variations. Johnstech claims that two self-cleaning features enable the Pad ROL 200K to deliver the lowest Kelvin contact resistance available on the market. Its oxide-removal wipe action prevents surface debris from accumulating on the force-contact tip. In addition, the socket's force and sense contacts work in combination to remove debris build-up between the two contacts.

Johnstech International, www.johnstech.com.

Generator helps support WiFi, radar coexistence

VeriWave's new RF Interference and DFS Pulse Generator system lets developers of 802.11n-compliant WiFi chipsets, receivers, APs (access points), and user devices expand test coverage, reduce development cycles, and reduce the cost and complexity of testing. The generator speeds the development of products that comply with new rules for WiFi devices sharing radio bands with Bluetooth devices, microwave ovens, and civilian radar installations.

Rather than requiring multiple signal generators to handle MIMO test capabilities, the RF Interference and DFS Pulse Generator system makes use of a VeriWave 802.11n WaveBlade instrument, which supports three spatial signal streams. VeriWave's interference generator simplifies the creation of interfering waveforms in popular 802.11 bands to a point-and-click process, allowing testers to configure and modify traffic characteristics including signal strength, burst lengths, and burst rates while automating and repeating tests.

Base price: $8995. *VeriWave, www.veriwave.com.*

Aeroflex rolls out portable RF radio-altimeter test set

Aeroflex claims that its ALT-8000 is the world's first RF-based portable radio-altimeter flightline test set. The universal test set provides full

RF loop testing for 4.3-GHz FMCW (frequency-modulated continuous-wave) radio altimeters and pulse radio altimeters.

Outfitted with a 12-in. color touch screen, the compact test set can be used to test radio altimeters installed in aircraft and unmanned aerial vehicles. It can be directly coupled to the radio altimeter Tx/Rx ports or con-

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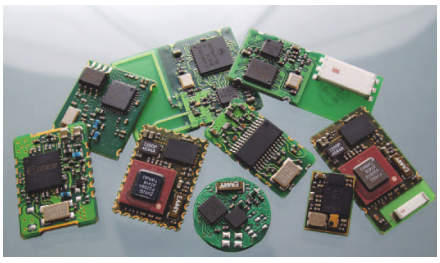
RF MODULES



Panasonic Electronic Components provides flexible, cost-effective RF modules for a variety of wireless personal-area-network applications. Extended range products featuring small footprints combined with network firmware flexibility are available in 802.15.4, Bluetooth, ISM, and new RPA (relative position awareness) hardware technologies.
Panasonic, www.panasonic.com/indcomp/rf.

Test & Measurement World's ANNUAL BUYER'S GUIDE

Our 2010 Buyer's Guide contains more than 60 product and service categories, divided into five main sections. Each section includes hotlinked vendor names and a sampling of products from the past year. If you'd like more information about advertising in the *Test & Measurement World* 2010 Buyer's Guide, please e-mail Judy Hayes at judith.hayes@cancom.com or phone (800) 438-6597. **www.tmworld.com**

nected via the supplied Tx/Rx antenna couplers, which accommodate most aircraft-antenna variants.

The ALT-8000 performs RF simulation of radio altitude from –100 ft to +50,000 ft, accurate to within ±1.5 ft. You can set the altitude rate to provide smooth ramping altitude simulation to verify decision heights and altitude trips. Up to three ALT-8000 test sets can be linked via an altitude sync line for executing two-channel or three-channel coordinated altitude simulation for dual-installation or triple-installation auto-land-system testing. The RF looped test verifies Tx frequency, power, and sweep rate.

Price: $15,000. *Aeroflex, www.aeroflex.com.*

LMS enhances noise-test software

Revision 10A of LMS International's Test.Lab integrated software environment for noise and vibration testing performs time-domain TPA (transfer-path analysis) and MIMO RF testing and also offers new capabilities for acoustic testing.

Time-domain TPA complements Test.Lab's frequency-domain TPA and is useful for analyzing transient phenomena. MIMO RF testing extends the modal testing techniques of Test.Lab and allows users to specify their excitation signals, define a shaped amplitude spectrum, and extend the application to multisine excitation.

For engineers who perform acoustic tests, the software's Sound Quality measurement feature has been expanded with new psycho-acoustic metrics used in the automotive and aerospace sectors, while the Sound Intensity feature gained a 3-D acoustic mesh generator. The software provides an overview of all measured and processed data, quality indicators, and related components to help users analyze the data for sound power, source ranking, and sound source localization.

LMS International, www.lmsintl.com.

Hamamatsu introduces scientific CMOS camera

Intended for low-light imaging at high frame rates, the ORCA-Flash2.8 digital camera from Hamamatsu leverages a scientific CMOS image sensor that achieves a resolution of 2.8 Mpixels. A combination of high speed, low noise, and ease of interface with external peripheral equipment makes the camera suitable for a wide variety of applications, such as semiconductor inspection, industrial imaging, and sensitive analytical measurements.

The ORCA-Flash2.8 delivers 45 fps at a full resolution of 1920x1440 pixels. In addition, the camera achieves a maximum frame rate of 1273 fps in subarray mode. The FL-280 cooled CMOS image sensor keeps readout noise minimal at just 3 electrons, even at very fast readout speeds.

Other features of the ORCA-Flash2.8 camera include an on-chip microlens and a high dynamic range of 4500:1, as well as on-chip analog gain and correction functions. External trigger functions and timing output functions ensure proper timing control with peripheral equipment. A Camera Link Base configuration interface is standard.

Hamamatsu Photonics, www.hamamatsu.com.

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VIEWPOINT

[An exclusive interview with a technical leader]

MICHAEL VOHRER
President and CEO
Rohde & Schwarz
Munich, Germany

Michael Vohrer studied communications engineering and began his professional career at Rohde & Schwarz in 1975. Starting as a development engineer, he rose to become head of the Test and Measurement Division in 1996, responsible for the marketing, design, and development of T&M instruments and systems. In 2003, Vohrer became a member of the executive board and was appointed president and COO, in charge of the Broadcasting, Test and Measurement, Radiocommunications Systems, and Radiomonitoring and Radiolocation Divisions. In January 2006, he became CEO of the company, which employs 7400 people in more than 70 countries.

Contributing editor Larry Maloney spoke with Michael Vohrer about trends in communications test in a recent telephone interview.

One-box solutions score with engineers

Q: Rohde & Schwarz celebrated its 75th anniversary in 2008. What factors have sustained the company during that long history?

A: There are two important factors from my viewpoint. First, we have continually expanded our portfolio of test and measurement products to offer a full basket of solutions for a wide variety of applications. And we've done this while meeting the customers' budget requirements. Second, we have established subsidiaries all over the world to be closer to the market and to support our customers. Currently, we have subsidiaries headed by our own people in more than 70 countries.

Q: What applications will be the biggest growth drivers for Rohde & Schwarz in 2010?

A: One of the biggest growth drivers now for our Test and Measurement Division is LTE technology. We see a big demand for the higher data rates in the wireless communications world offered by LTE. There's great potential for implementation of LTE in hundreds of existing cellular networks all over the world.

Q: How did the global recession change your company's product development and strategies?

A: Like many companies, we implemented cost-cutting measures at a very early stage, and that helped get us through the crisis. We had to lay off only a few people, and managed to strengthen our R&D teams to bolster our product portfolio. Recessions last for a limited time, and it is more important to concentrate on preparing your company for the business recovery.

Q: Isn't it becoming more important to offer affordable test and measurement solutions?

A: Our aim, especially during tough economic times, is to offer customers the best price-to-performance ratio. Increasingly, we achieve this goal by integrating all required test and measurement functions into one instrument. This allows you to perform necessary applications without any additional instruments, while offering fully automatic measurement routines. Our "one-box" solutions interact with the devices under test in real time in applications that are often not possible with single instruments. They are also more economical. Among the many examples of our one-box products are the R&S DVSG digital video signal generator and the CMU and CMW radio communications testers for mobile phone development and production.

Q: What were your most significant product introductions of the past year?

A: One of the most important developments is not an actual instrument but the ability of all our instruments to comply with the new LTE standard. This is essential to supporting customers in developing base and mobile stations. Moving to specific instruments, there's the new R&S ETL, a multistandard platform for the analysis of TV signals. It combines TV test receiver and spectrum analyzer functionality in a single unit, while providing high measurement accuracy. It's a "just in time" product that addresses the transition from the analog to digital TV world. Another new key product is our portable receiver, the R&S PR100. Featuring an internal spectrum analyzer, this compact instrument detects signals up to 7.5 GHz for such diverse applications as radio reconnaissance, locating interference sources, and frequency monitoring. Combined with our portable handheld antennas, the instrument serves as a direction finder, with an integrated GPS receiver that shows not only where the signal is coming from but also the location of an interferer. T&MW

Michael Vohrer talks more about communications test and product development in the online version of this interview: www.tmworld.com/2010_05.

To read past Viewpoint columns, go to www.tmworld.com/viewpoint.

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